PFM Step-up DC/DC Converter & Voltage Detector

Features

- High output voltage accuracy: ±5%
- Low ripple and low noise
- Low start-up voltage (when the output current is 1mA): 0.95V
- Low current consumption: 14μA with 1.5V input (typ.)
- Fixed output voltage: 2.7V
- Built-in 2.1V (typ.) voltage detector
- 8-pin SOP package

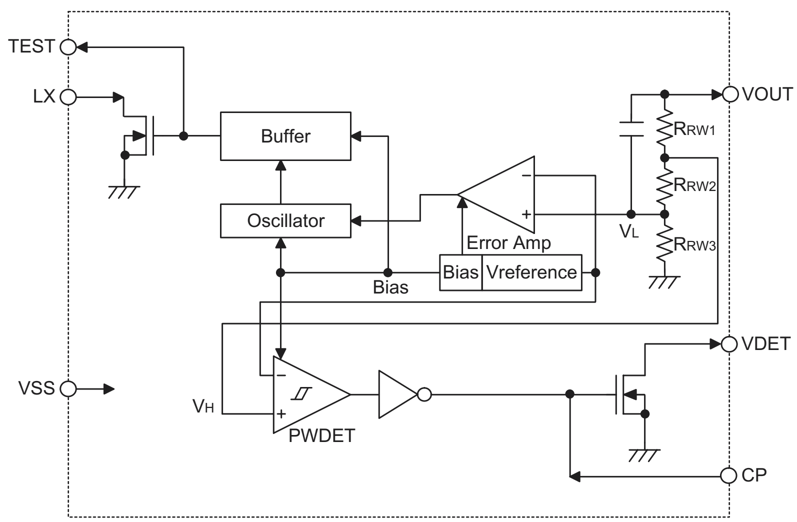
Applications

- Pager
- RF Mouse/Keyboard

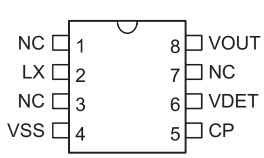
General Description

The HT7627 DC/DC converter with built-in voltage detector is a high performance CMOS IC, suitable for use in battery-powered system application with low noise and low supply current. The HT7627 consists of two major parts, one is DC/DC converter and the other is voltage detector. The DC/DC converter part consists of reference voltage source, error amplifier, control transistor, oscillation circuit and output voltage setting resistor. The voltage detector part consists of a high-precision and low power consumption standard voltage source, a comparator, hysteresis circuit and an output driver. As external parts, a coil, a diode, and a capacitor are available for obtaining a constant output (2.7V) higher than the input voltage for the DC/DC converter part.

Block Diagram



Pin Assignment



HT7627
– 8 SOP-A

Pin Description

Pin No.	Pin Name	I/O	Description
1, 3, 7	NC	—	No connection
2	LX	I	Switching pin
4	VSS	—	Negative power supply, ground
5	CP	I	External capacitor for adjusting VDET output delay time.
6	VDET	O	Voltage detector open drain output (needs a pull-high resistor)
8	VOUT	O	DC/DC converter voltage output

Absolute Maximum Ratings

Supply Voltage .... V_{SS}–0.3V to V_{SS}+6V

Switching pin Voltage .... V_{SS}–0.3V to V_{SS}+6V

Power Consumption 150mW

Storage Temperature .... –40°C to 125°C

Operating Temperature .... –25°C to 70°C

Note: These are stress ratings only. Stresses exceeding the range specified under "Absolute Maximum Ratings" may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

Electrical Characteristics

Ta=25°C, V_{OUT}=2.7V

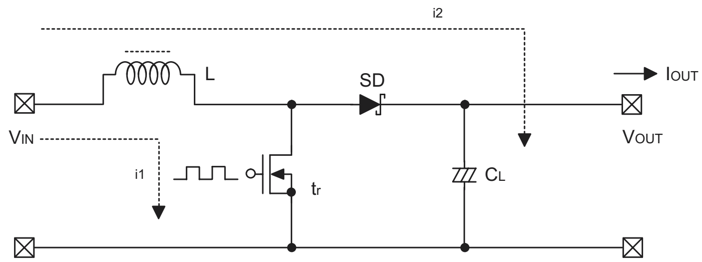
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{OUT}	Output Voltage	—	2.56	2.7	2.75	V
V_{IN}	Input Voltage	—	—	—	5	V
Vstart	Starting Voltage	L=330μH, I_L=1mA	—	0.95	1.1	V
Vhold	Voltage Hold	—	0.9	—	—	V
Iin	Current Consumption	Measure at no load	—	14	20	μA
I_{LX}	LX Switching Current	V_{IN}=1.5V	60	—	—	mA
I_{LEAK}	LX Leakage Current	—	—	—	1	μA
f_{OSC}	Oscillator Frequency	V_{IN}=1.5V	—	139	—	kHz
V_{DET}	H→L Detectable Voltage	—	2.0	2.1	2.2	V
	L→H Detectable Voltage	—	2.2	2.3	2.4	V
V_{HYS}	Hysteresis Width	—	—	0.2	—	V
I_{DETOL}	V_{DET} Output Sink Current	V_{OUT}=2.2V, V_{DET}=0.2V	0.5	—	—	mA

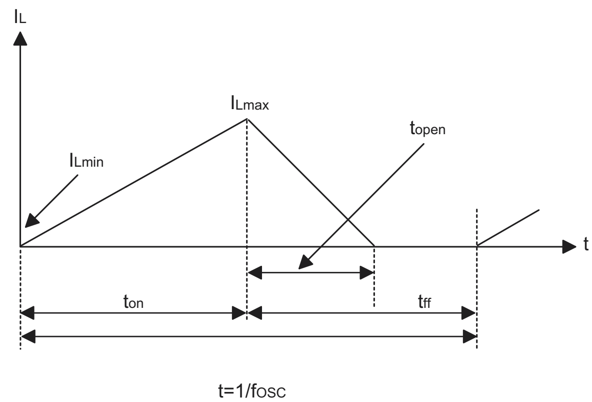
Functional Description

Operation of step-up DC/DC converter

The following figures show the basic circuit configuration of the step-up operation of the IC. In the configuration, when the transistor tr is entirely Off, the output voltage is the value of the input voltage V_{IN} minus the voltage reduced by inductor L and Schottky diode SD. When tr has been On for time ton and is suddenly turned Off, voltage V_L is generated at the edges of L because of the energy accumulated during the ton period. Therefore, the peak value of the voltage generated at that time is V_{IN}+V_L, and it is stored in the output capacitor C_L via SD. This generates the step-up output voltage V_{OUT} that is larger than V_{IN}.

The operation will be explained with reference to the following diagrams:





Step1: t_r is turned ON and current I_L (=i1) flows, so that energy is charged in L. At this moment, I_L (=i1) is increased from I_{Lmin} to reach I_{Lmax} in proportion to the on-time period (t_{on}) of t_r.

Step2: When t_r is turned OFF, Schottky diode (SD) is turned ON in order that L maintains I_L at I_{Lmax}, so that current I_L (=i2) is released.

Step3: I_L (=i2) is gradually decreased, I_L reaches I_{Lmin} after a time period of t_{open}, so that SD is turned OFF. t_r will be turned ON in the next cycle.

In the case of PWM control system, the output voltage is maintained constant by controlling the on-time period (t_{on}), with the oscillator frequency (f_{OSC}) being maintained constant.

Voltage detector operation

The HT7627 built-in voltage detector is equipped with a high stability voltage reference which is connected to the negative of a comparator — denoted as Vref in the following figure for NMOS output voltage detector.

When the voltage drop to the positive input of the comparator (i.e. V_B) is higher than Vref, V_{OUT} goes high, and V_B is expressed as $V_{BH}=V_{DD} \times (R_B+R_C) / (R_A+R_B+R_C)$. If V_{DD} is decreased so that V_B falls to a value less than Vref, the comparator output inverts from high to low, V_{OUT} goes low, V_C is high, RC is bypassed, and V_B becomes: $V_{BL}=V_{DD} \times R_B/(R_A+R_B)$, which is less than V_{BH}. By so doing, the comparator output will remain low to prevent the circuit from oscillating when $V_B \approx$Vref.

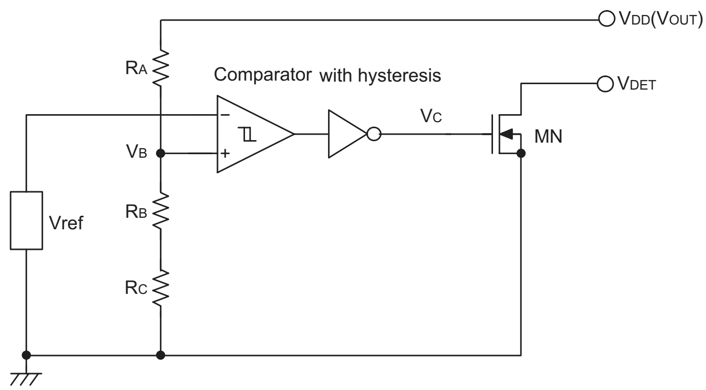
If V_{DD} falls below the minimum operating voltage, the output becomes undefined. When V_{DD} goes from low to $V_{DD} \times R_B / (R_A+R_B) >$ Vref, the comparator output and V_{OUT} goes high. The detectable voltage is defined as:

$$V_{DETECT}(-)= \frac{RA + RB + RC}{RB + RC} \times Vref$$

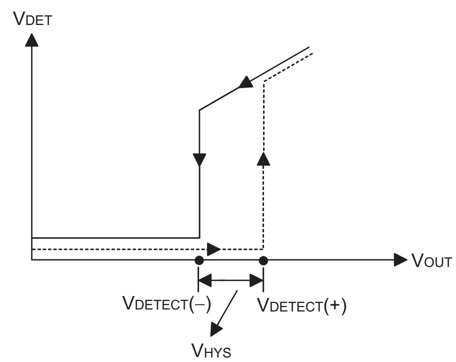
The release voltage is defined as:

$$V_{DETECT}(+)= \frac{RA + RB + RC}{RB} \times Vref$$

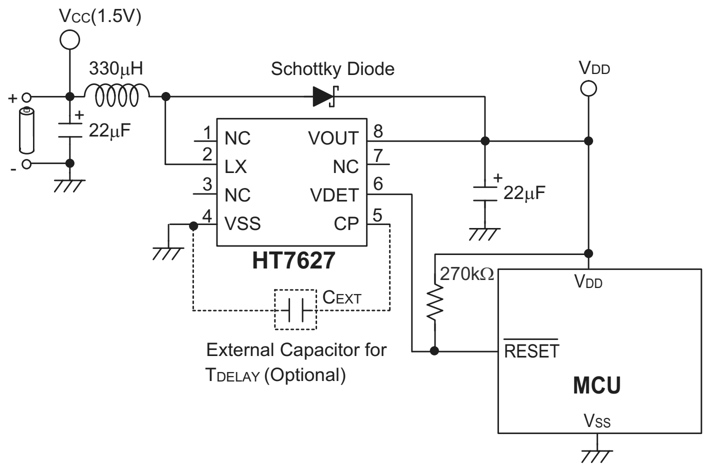
The hysteresis width is $V_{HYS}= V_{DETECT}(+) - V_{DETECT}(-)$



The following figure shows the hysteresis effect according to the previous figure.



Application Circuits



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