High Efficiency Synchronous Step-Up DC/DC Converter

Features

- Low start-up voltage: 0.7V (Typ.)
- High efficiency: HT77S10: 91% (Typ.) at I_{OUT}=200mA, V_{IN}=2.4V, V_{OUT}=3.3V
- High output voltage accuracy: ±4%
- Output voltage: 3.3V, 5.0V or Adjustable
- Low ripple and low noise
- Ultra low supply current: 20μA (Typ.)
- Low shutdown current: 1μA (Max.)
- Built-in voltage detector
- 8-pin MSOP/SOP packages

Applications

- Battery-powered equipment power source
- Power source for cameras, camcorders, VCRs, PDAs, pagers, electronic data banks, and hand-held communication equipment
- Power source for appliances, which require a higher operating voltage than that of the application batteries

General Description

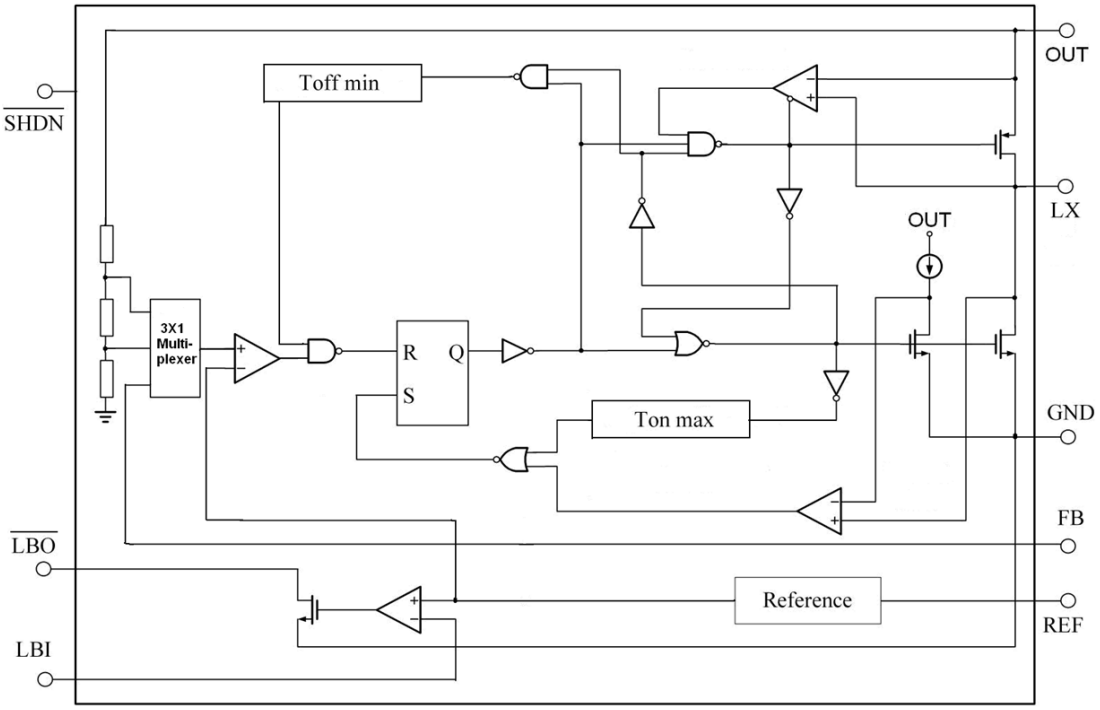
The HT77S11 and HT77S10 are high efficiency PFM synchronous step-up DC-DC converters. The two devices although functionally similar are different in their output drive current capabilities. Synchronous rectification operation is used to increase device efficiency and to reduce the external component resulting in reduced product costs. The converter switching frequency, which can have a value up to 500KHz, will vary according to the load demands and according to the input voltage to keep the output voltage at the required level.

The HT77S11 and HT77S10 have 0.7V start-up voltage, and will consume a typical quiescent current of 20μA. A shutdown mode is provided whereby the operating current will be reduced a very low value. The output voltage has two fixed voltages of 3.3V by setting FB to OUT pin and 5V by setting FB to GND pin, but can also be adjusted between a value of 1.8V~5.5V using two external resistors. With internal voltage detector function, the detected voltage can be set by using dividing resistor.

Selection Table

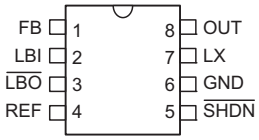
Part No.	Current Limit	Package
HT77S10	1.0A	8MSOP/SOP
HT77S11	0.55A	

Block Diagram



Note: * The FB pin is connected to an external resistive divider, OUT or GND pins to set the output voltage.

Pin Assignment



HT77S10/HT77S11
8 MSOP-A/SOP-A

Pin Descriptions

Pin No.	Pin Name	Description
1	FB	Feedback Input Pin. This pin is used to select the required output voltage. It can be connected to an external resistor divider for a user selected voltage or to either the OUT or GND pins for a fixed voltage. GND: 5V output OUT: 3.3V output Resistor Divider: 1.8V~5.5V range output
2	LBI	Low-Battery Comparator Input Pin. This pin is connected to the internal low battery voltage comparator. If the voltage on this pin is less than the REF voltage - nominally 1.3V - then the $\overline{LBO}$ output will be low.
3	$\overline{LBO}$	Open-Drain Low Battery Comparator Output. This pin is used to indicate a low battery condition and is connected to the low battery voltage comparator output. Note that the pin will be in a high impedence condition when the device is in the shutdown mode. High Z: $V_{LBI} > V_{REF}$ 0: $V_{LBI} < V_{REF}$
4	REF	Reference Voltage Output Pin. This pin is the output from the voltage reference generator and should be connected to a 0.1μF bypass capacitor.
5	$\overline{SHDN}$	Shutdown Input Pin. This pin is used to power down the device and place it into the shutdown mode. High: Device in normal operating mode Low: Device in shutdown mode
6	GND	Ground Pin.
7	LX	Switching Output Pin. This pin is the device switching output pin which is connected to the internal N-channel and P-channel switching power MOSFET drain pins.
8	OUT	Power Output Pin. This pin is the converter output pin. It also supplies bootstrap power to the device.

Absolute Maximum Ratings

Supply Voltage .....–0.3V to 7.0V

Storage Temperature .....–50°C to 125°C

Operating Temperature .....–40°C to 85°C

Note: These are stress ratings only. Stresses exceeding the range specified under "Absolute Maximum Ratings" may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

Electrical Characteristics

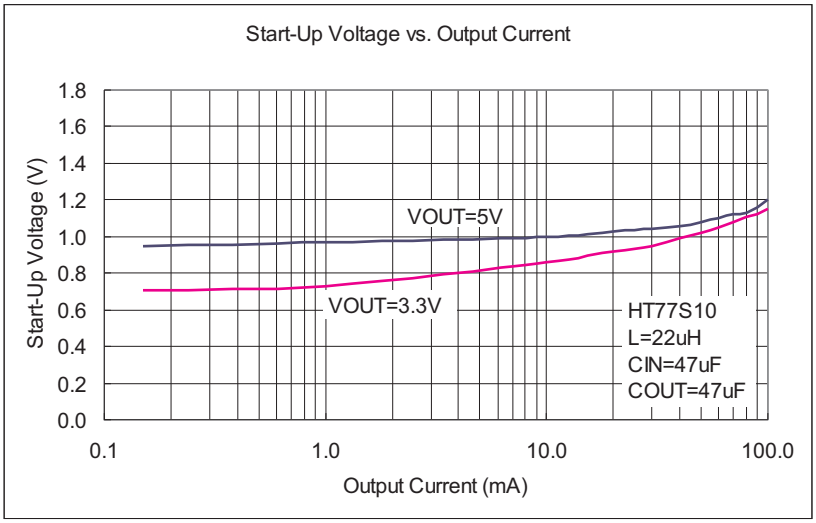
V_{IN}=2V, $\overline{SHDN}$=FB=OUT, V_{OUT}=3.3V, refer to figure 1 unless otherwise specified, Ta=25°C

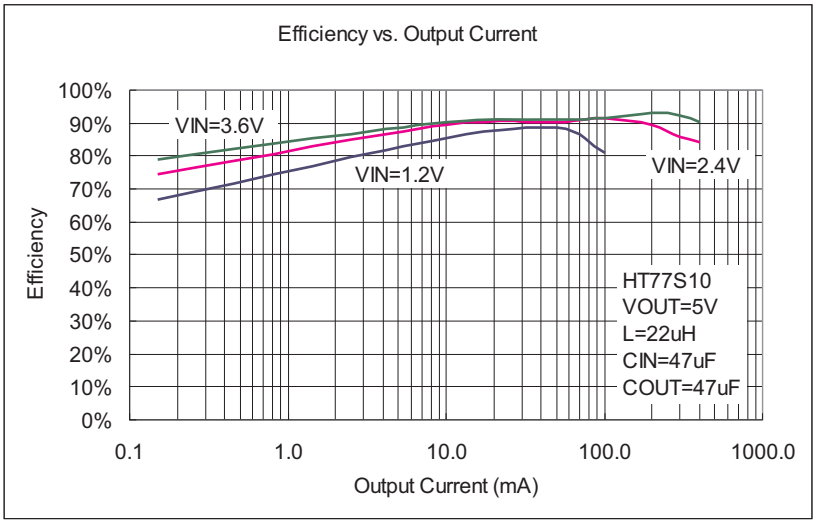
Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
V_{IN}	Operating Input Voltage	—		—	—	5.5	V
V_{IN-MIN}	Minimum Input Voltage	—		—	0.7	—	V
$V_{IN-START}$	Start-up Input Voltage	R_L=3kΩ		—	0.7	0.9	V
V_{OUT}	Output Voltage	FB=OUT		3.17	3.30	3.43	V
		FB=GND		4.80	5.00	5.20	V
		V_{IN} < V_{OUT}, FB using two external resistors		1.80	—	5.50	V
V_{REF}	Reference Voltage	I_{REF}=0		1.268	1.300	1.333	V
$V_{REF-LOAD}$	Reference Load Regulation	I_{REF}=0 to 150μA		—	10	30	mV
$V_{REF-LINE}$	Reference Line Regulation	V_{OUT}= 2V to 5.5V		—	5	10	mV/V
$R_{DS(ON)}$	Internal PMOS and N-MOS On Resistance	I_L=100mA		—	0.3	—	Ω
I_{LIM}	Internal NMOS Switch Current Limit	HT77S10		0.80	1.00	1.20	A
		HT77S11		0.40	0.55	0.75	A
I_{LEAK}	Internal N-MOS Leakage Current	V_{LX}=4V, V_{OUT}=5.5V		—	0.05	1.00	μA
I_{OUT}	Steady-State Output Current	FB=OUT	HT77S10	300	350	—	mA
			HT77S11	150	300	—	mA
		FB=GND	HT77S10	180	230	—	mA
			HT77S11	90	160	—	mA
I_Q	Quiescent Current	V_{FB}=1.4V, V_{OUT}=3.3V		—	20	35	μA
V_{FB}	FB Input Threshold	—		1.268	1.300	1.333	V
V_{LBI}	LBI Input Threshold	—		1.268	1.300	1.333	V
$V_{\overline{LBO}}$	$\overline{LBO}$ Low Output Voltage	V_{LBI}=0, I_{SINK}=1mA		—	0.2	0.4	V
$I_{\overline{LBO}}$	$\overline{LBO}$ Off Leakage Current	$V_{\overline{LBO}}$ =5.5V, V_{LBI}=5.5V		—	0.07	1.00	μA
$I_{\overline{SHDN}}$	Shutdown Current	$\overline{SHDN}$=GND		—	0.1	1	μA
V_{IH}	$\overline{SHDN}$ Pin Voltage High	—		1.5	—	—	V
V_{IL}	$\overline{SHDN}$ Pin Voltage Low	—		—	—	0.4	V
$t_{ON(MAX)}$	LX Switch On Time	V_{FB}=1V, V_{OUT}=3.3V		2	4	7	μs
$t_{OFF(MIN)}$	LX Switch Off Time	V_{FB}=1V, V_{OUT}=3.3V		0.6	0.9	1.4	μs
η	Efficiency	V_{OUT}=3.3V, I_O=200mA		—	90	—	%
		V_{IN}=1.1V,V_{OUT}=2.0V, I_O=1mA		—	85	—	%

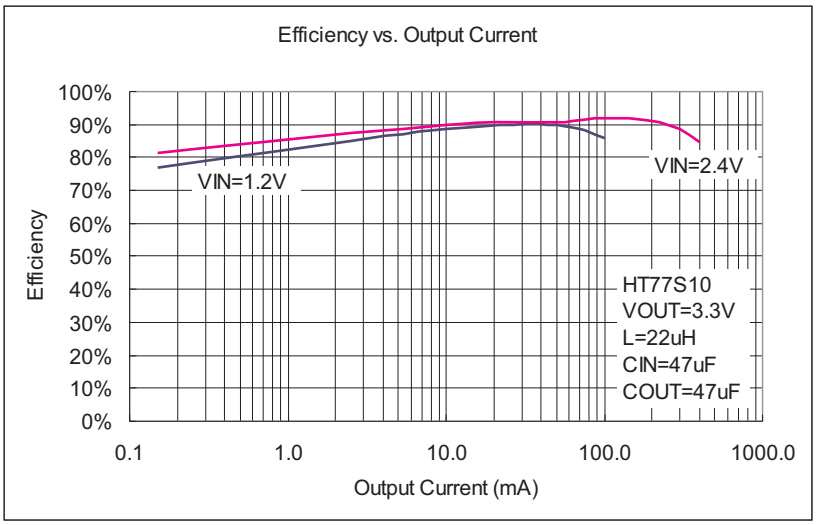
Note: Absolute maximum ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. The guaranteed specifications apply only for the test conditions listed.

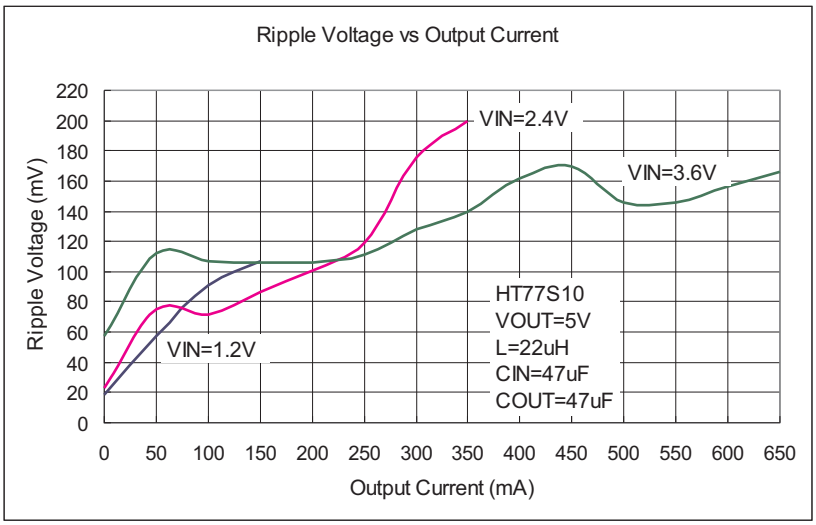
Specifications are production tested at Ta=25 degree. Specifications over -40 to 85 degree operating temperature range are assured by design.

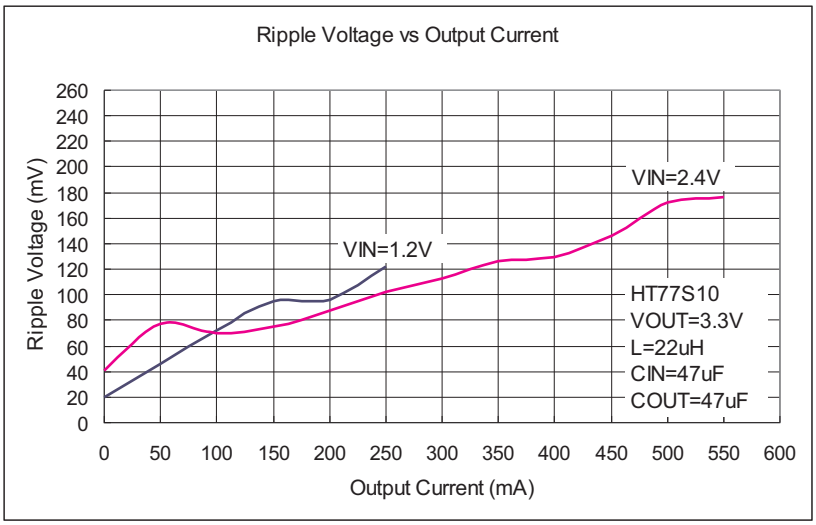
Typical Performance Characteristics








Ripple Voltage vs Output Current
Ripple Voltage (mV)
220
200
180
160
140
120
100
80
60
40
20
0
0 50 100 150 200 250 300 350 400 450 500 550 600 650
Output Current (mA)
VIN=2.4V
VIN=3.6V
VIN=1.2V
HT77S10
VOUT=5V
L=22uH
CIN=47uF
COUT=47uF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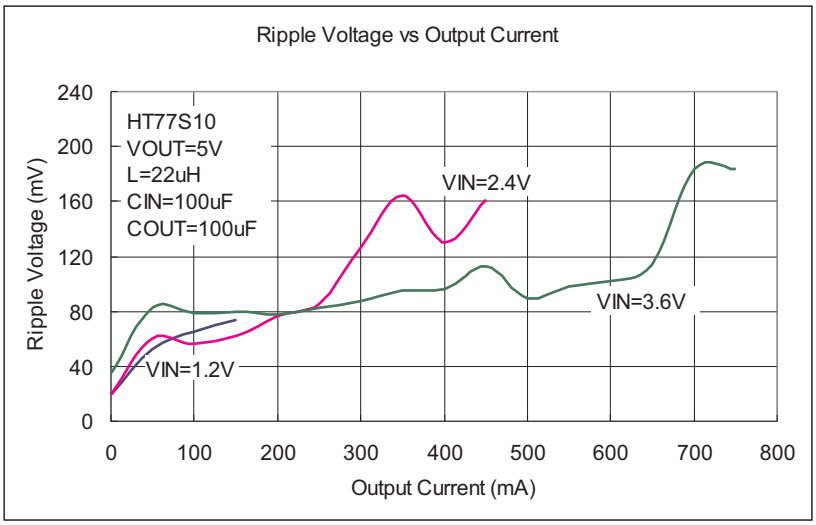
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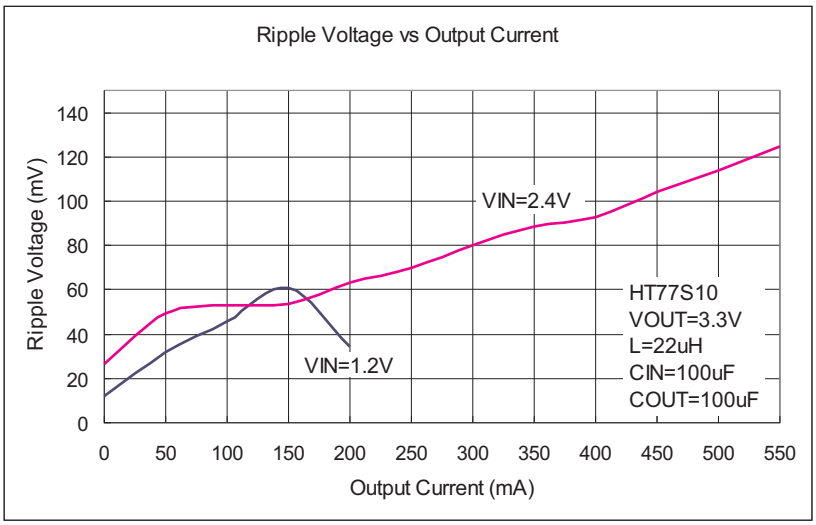


Functional Description

These devices use minimum off-time, current limited pulse-frequency modulation, PFM, techniques for output voltage regulation. The PFM control circuitry acts to control the energy stored in an external inductor to regulate the output voltage to the correct level. Using PFM for control offers the advantages of very low quiescent currents.

The device output voltage is continuously monitored using an internal comparator. The output status of the comparator is then used to determine what action the control logic should take to correct any differences between the actual output voltage and the required voltage. The variable switching frequency depends upon the input voltage and the load demands but can have a frequency of up to 500kHz. The maximum current of the internal NMOS power switching transistor is fixed at 1A for the HT77S10 and 0.55A for the HT77S11.

The switching frequency is controlled by two internal single shot circuits that generate pulses of 0.9μs typical minimum off-time and 4μs typical maximum on-time. If the circuitry detects that the output voltage is lower than the required voltage, the control circuitry will ensure that more inductor energy is transferred to the load. Refer to the block diagram to see how this regulation is implemented using the following two ON and OFF steps:

- ON Step
  During this step, the NMOS transistor will be switched on which effectively connects the LX pin to ground, and allows energy to build up in the inductor as supplied by VIN. Inductor energy build up is allowed to continue until the inductor current reaches a maximum of 1A for the HT77S10 and 0.55A for the HT77S11 or if the on time exceeds 4μs.
- OFF Step
  The energy stored in the inductor during the ON Step is now transferred to the load via the synchronous switch for a minimum time of 0.9μs. When the output voltage is less than the required regulated voltage the synchronous switch will switch off which will reduce the inductor current to zero. It is during this cycle that the PMOS power transistor is switched on which shunts its body diode, resulting in enhanced conversion efficiency.

As the design of these devices uses an internal synchronous rectifier, there is no requirement to provide the usual external Schottky diode. This gives users the advantage of smaller circuit board areas and reduced costs.

Low Voltage Start-up

These devices can provide a very low start up voltage down to 0.7V. When power is first applied, the synchronous switch will be initially off but energy will be transferred to the load through its intrinsic body diode.

Voltage Reference

The internal voltage reference circuit supplies a nominal voltage of 1.3V on the REF pin. Up to 150μA can be sourced on this pin for use by external circuits. The reference voltage provided here offers excellent load regulation characteristics, however a bypass capacitor of 0.1μF should be connected for proper operation.

Shutdown

During normal device operation, the SHDN pin should be either high or connected to the OUT pin. When the device is in the shutdown mode, that is when the SHDN pin is pulled low, the internal circuitry will be switched off, thus reducing the current demands on the VIN power source. During shutdown, the PMOS power transistor body diode will allow current to flow from VIN to VOUT, therefore VOUT falls to a value of approximately VIN - 0.6V.

Low Battery Detection

A low battery detector function is provided in the device using an internal comparator. The output pin LBO is the output and input pin LBI is the input for this function. As this is an open-drain NMOS type output, it is usually necessary to connect an external pull-high resistor for proper use. This pin can be pulled-high up to a voltage of 6V independently of the OUT pin voltage. When the voltage on LBI is higher than the threshold voltage, the LBO output will be high impedance. If the low battery detection function is not used, the LBI and LBO pins should be grounded. The LBI threshold voltage is set using two external resistors, R3 and R4. The R3 and R4 ratio can be calculated using the following equation. See Figure.1, Figure.2 and Figure.3:

$$\frac{R3}{R4} = \frac{V_{IN}}{V_{REF}} - 1$$

Where

V_{IN} = Input Voltage, $V_{IN} > V_{REF}$
Reference Voltage V_{REF} = 1.3V

Application Information

Output Voltage Selection

The required output voltage is controlled using the FB pin. Two fixed voltages of 3.3V and 5V are available or an adjustable output voltage which is set using an external resistor divider.

VOUT	FB pin
3.3V	Connect OUT
5.0V	Connect to GND
1.8V≤VOUT≤5.5V	Connect to resistive divider (Figure.3) $V_{OUT}= V_{REF} (1+ \frac{R1}{R2})$

Where

V_{REF}= Reference Voltage is 1.3V

A recommended value for R2 is 240kΩ.

Inductor Selection

Selecting a suitable inductor is an important consideration as it is usually a compromise situation between the output current requirements, the inductor saturation limit and the acceptable output voltage ripple. Lower values of inductor values can provide higher output currents but will suffer from higher ripple voltages and reduced efficiencies. Higher inductor values can provide reduced output ripple voltages and better efficiencies, but will be limited in their output current capabilities. For all inductors it must be noted however that lower core losses and lower DC resistance values will always provide higher efficiencies.

The peak inductor current can be calculated using the following equation:

$$I_{L(PEAK)} = \frac{V_{OUT} \times Io}{V_{IN} \times \eta} + \frac{V_{IN} \times (V_{OUT} - V_{IN}) \times Ts}{2 \times V_{OUT} \times L}$$

Where

V_{IN} = Input Voltage
V_{OUT} = Output Voltage
I_O = Output Current
η = Efficiency
Ts = Period
L = Inductor

Capacitor Selection

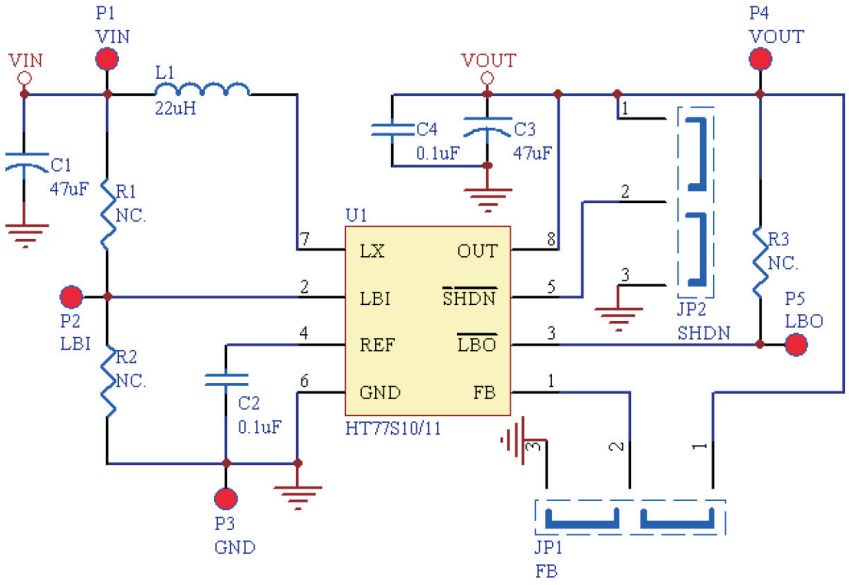
As the output capacitor selected affects both efficiency and output ripple voltage, it must be chosen with care to achieve best results from the converter. Output voltage ripple is the product of the peak inductor current and the output capacitor equivalent series resistance or ESR for short. It is important that low ESR value capacitors are used to achieve optimum performance. One method to achieve low ESR values is to connect two or more filter capacitors in parallel. The capacitors values and rated voltages are only suggested values.

Layout Guidelines

Good PCB layout is an extremely important factor is ensuring the optimum performance from switching regulator converters. Poorly thought out circuit layout can result in related noise problems. In order to minimise both EMI and switching noise, the follow guidelines should be followed:

- All tracks should be as short and wide as possible
- All components must be located as close to the IC as possible
- A star ground connection should be used to connect the input capacitor, C1, output capacitors, C3 and C4, and the IC GND pin
- Feedback resistors must be kept close as close to the FB pin as possible to limit the possibility of noise injection onto the PCB track connected to the FB pin
- A full ground plane will do much to enhance EMI performance

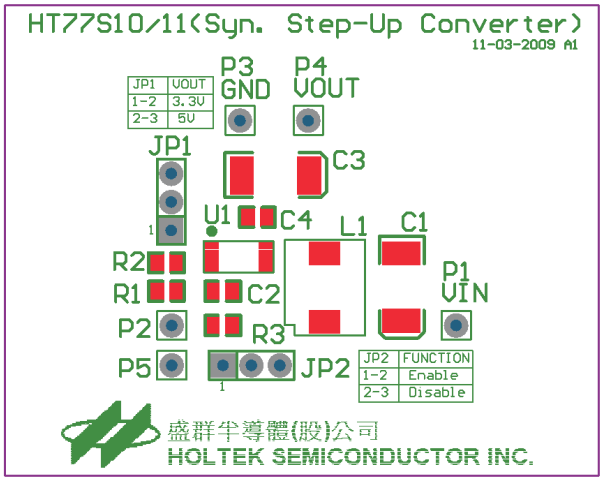
A demo board schematic and layout is provided for consultation below:



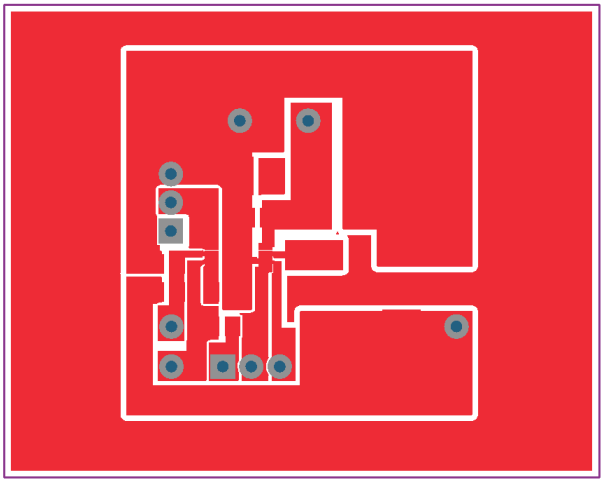
SHDN	Finction
1-2	Enable
2-3	Disable

LBI	LBO
>VREF	HIGH Z
<VREF	0

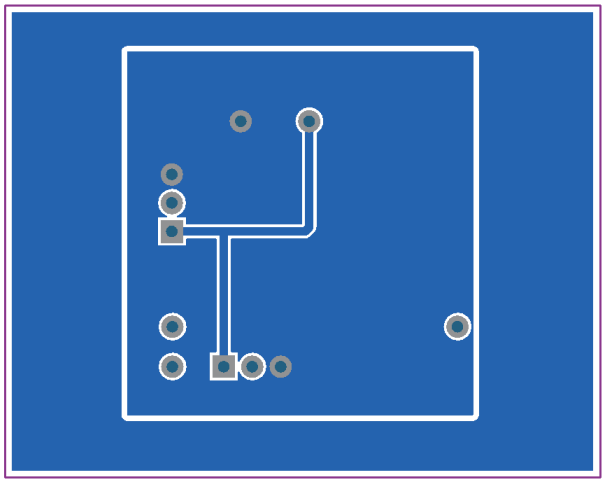
FB	VOUT
1-2	3.3V
2-3	5V



TopOverlay View



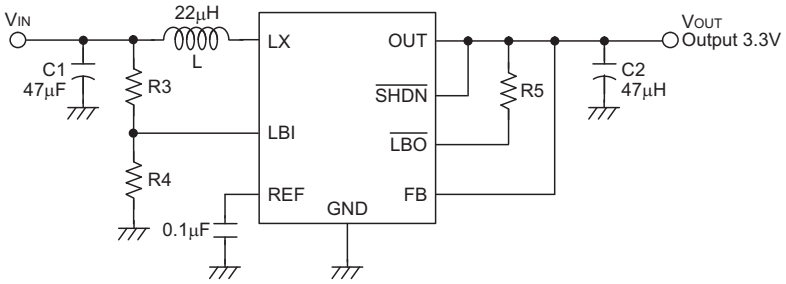
TopLayer View



BottomLayer View

Application Circuits

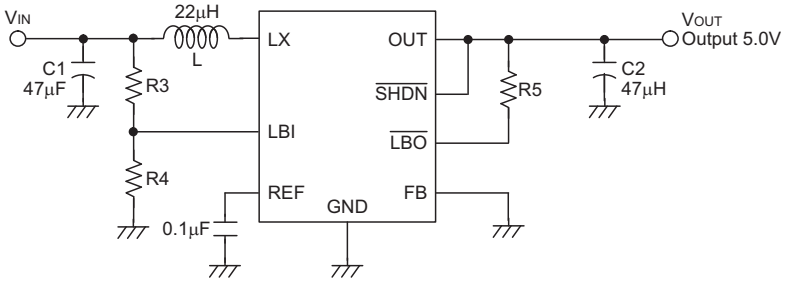
V_{OUT}=3.3V



L: TDK SLF7045T-220MR90-PF
C1, C2: Vishay 593D476X9016C2

Figure 1

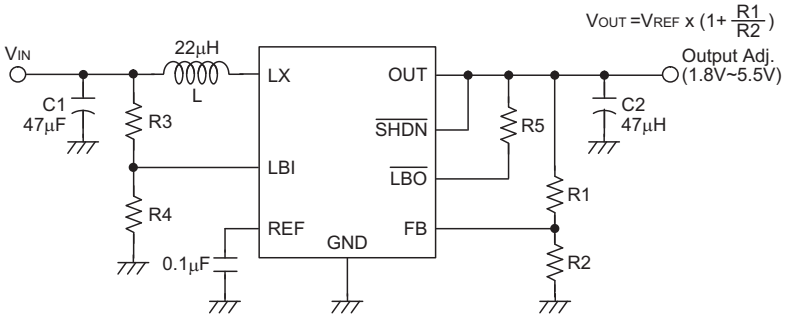
V_{OUT}=5.0V



L: TDK SLF7045T-220MR90-PF
C1, C2: Vishay 593D476X9016C2

Figure 2

V_{OUT}=1.8V~5.5V



L: TDK SLF7045T-220MR90-PF
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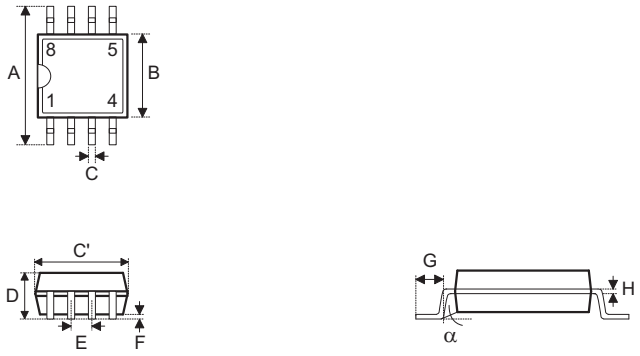
Figure 3

Package Information

8-pin SOP (150mil) Outline Dimensions

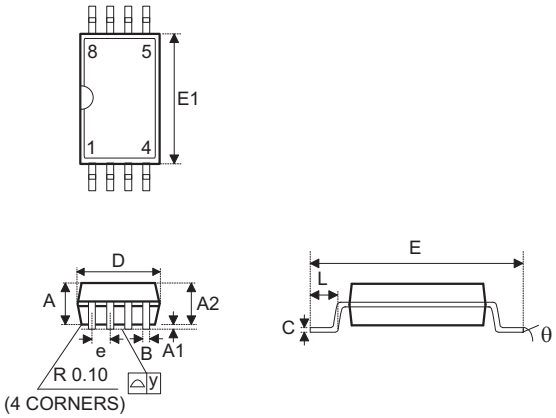


- MS-012

Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A	0.228	—	0.244
B	0.150	—	0.157
C	0.012	—	0.020
C′	0.188	—	0.197
D	—	—	0.069
E	—	0.050	—
F	0.004	—	0.010
G	0.016	—	0.050
H	0.007	—	0.010
α	0°	—	8°

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	5.79	—	6.20
B	3.81	—	3.99
C	0.30	—	0.51
C′	4.78	—	5.00
D	—	—	1.75
E	—	1.27	—
F	0.10	—	0.25
G	0.41	—	1.27
H	0.18	—	0.25
α	0°	—	8°

8-pin MSOP Outline Dimensions



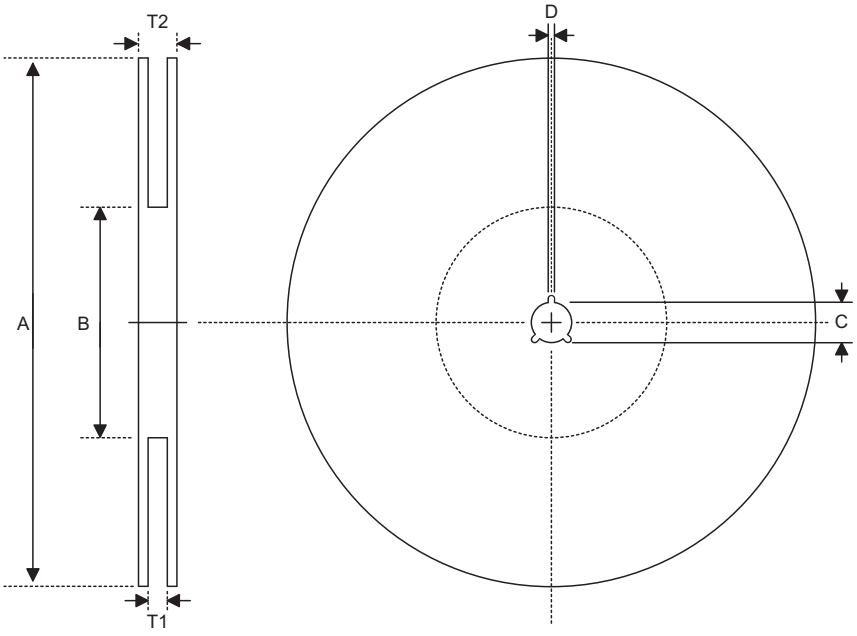
- MO-187

Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A	—	—	0.043
A1	0.000	—	0.006
A2	0.030	—	0.037
B	0.009	—	0.013
C	0.003	—	0.009
D	—	0.012	—
E	—	0.193	—
E1	—	0.118	—
e	—	0.026	—
L	0.016	—	0.031
L1	—	0.037	—
y	—	—	0.004
θ	0°	—	8°

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	—	—	1.10
A1	0.00	—	0.15
A2	0.75	—	0.95
B	0.22	—	0.33
C	0.08	—	0.23
D	—	3.00	—
E	—	4.90	—
E1	—	3.00	—
e	—	0.65	—
L	0.40	—	0.80
L1	—	0.95	—
y	—	—	0.10
θ	0°	—	8°

Product Tape and Reel Specifications

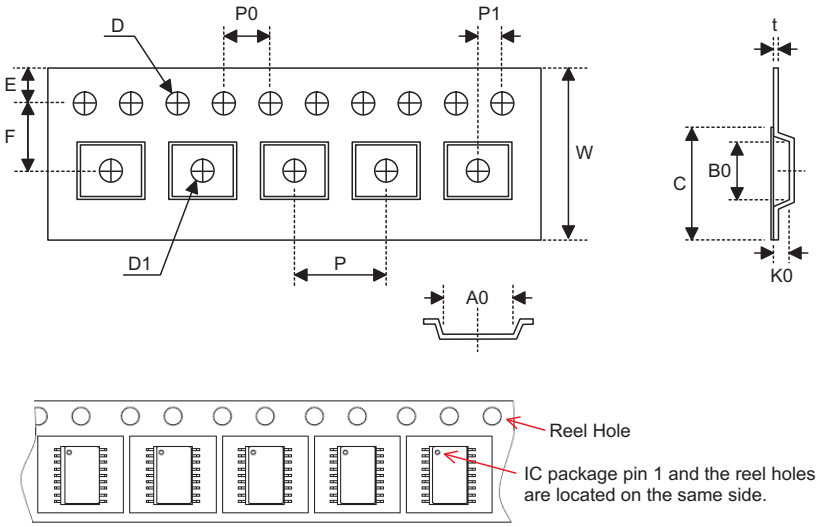
Reel Dimensions



SOP 8N

Symbol	Description	Dimensions in mm
A	Reel Outer Diameter	330.0±1.0
B	Reel Inner Diameter	100.0±1.5
C	Spindle Hole Diameter	13.0 $^{+0.5/-0.2}$
D	Key Slit Width	2.0±0.5
T1	Space Between Flange	12.8 $^{+0.3/-0.2}$
T2	Reel Thickness	18.2±0.2

Carrier Tape Dimensions



SOP 8N

Symbol	Description	Dimensions in mm
W	Carrier Tape Width	12.0 $^{+0.3/-0.1}$
P	Cavity Pitch	8.0±0.1
E	Perforation Position	1.75±0.1
F	Cavity to Perforation (Width Direction)	5.5±0.1
D	Perforation Diameter	1.55±0.1
D1	Cavity Hole Diameter	1.50 $^{+0.25/-0.00}$
P0	Perforation Pitch	4.0±0.1
P1	Cavity to Perforation (Length Direction)	2.0±0.1
A0	Cavity Length	6.4±0.1
B0	Cavity Width	5.2±0.1
K0	Cavity Depth	2.1±0.1
t	Carrier Tape Thickness	0.30±0.05
C	Cover Tape Width	9.3±0.1

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