Features

- Real Time Clock/Calendar Functions
  - Includes: Sec, Minutes, Hours, Day, Date, Month, and year in BCD format
- Clock operating voltage: 2.0V~5.5V
- Supply voltage V_{DD}=2.7V~5.5V
- Automatic leap year correction, valid until year 2099
- Automatic supply switch over
- Integrated oscillator load capacitors - CL=12.5pF
- Clock compensation
- Programmable alarm and interrupt function
- 15 selectable frequency outputs
- 4 Bytes EEPROM for user
- Serial commutation via I^2C or 3-wire interface
- 8-pin DIP, SOP and MSOP package for I^2C interface
- 10-pin MSOP package for 3-wire interface

Applications

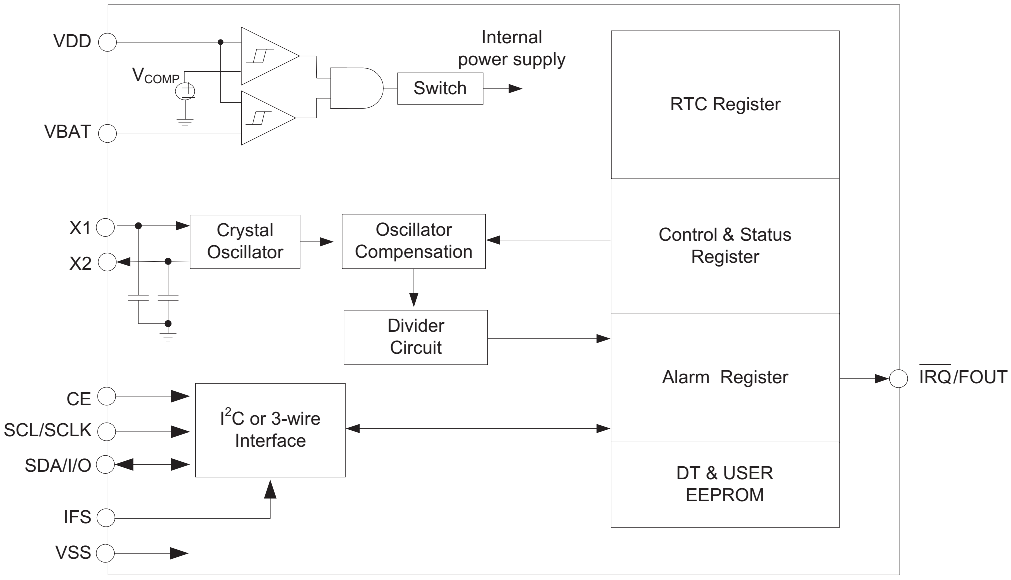
- Utility meters
- Consumer electronics
- Portable equipment
- Wireless equipment
- POS equipment
- Computer products
- Other industrial/Medical/Automotive applications

General Description

The HT1382 is a low power real time clock device with two serial interface: I^2C or 3-wire. The interface mode is selected by the chosen chip version. The device provides both clock and calendar information in BCD format and also includes alarm functions. The calendar is accurate until the year 2099 and includes automatic leap year correction.

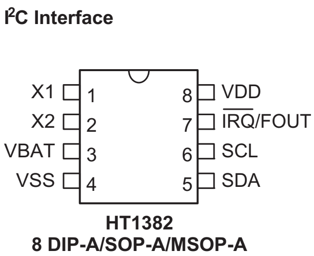
An external 32768Hz crystal is used as the device oscillator for device timing for which is provided an integrated crystal load capacitance of 12.5pF. The device includes a crystal oscillator temperature compensation function and internal power control circuitry detects power failures and automatically switches to the battery supply when a power failure occurs.

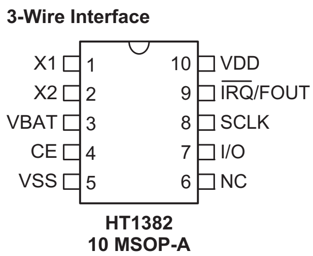
Block Diagram



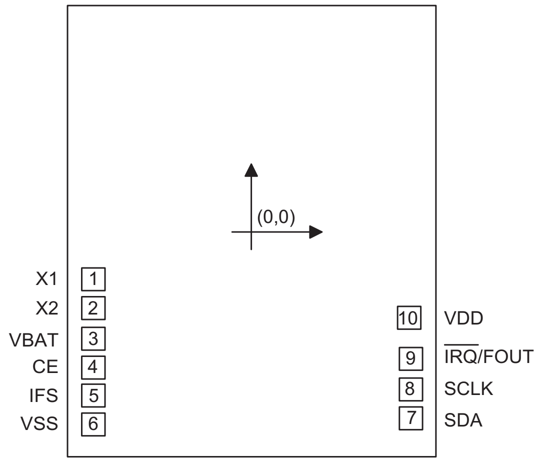
Note: IFS pin is used for selecting I^2C interface or 3-wire interface.
I^2C interface is selected when IFS is unconnected.
3-wire interface is selected when IFS is connected to VSS.

Pin Assignment





Pad Assignment



Chip size: 1245 × 1520 (μm)^2

* The IC substrate should be connected to VSS in the PCB layout artwork.

Pad Coordinates

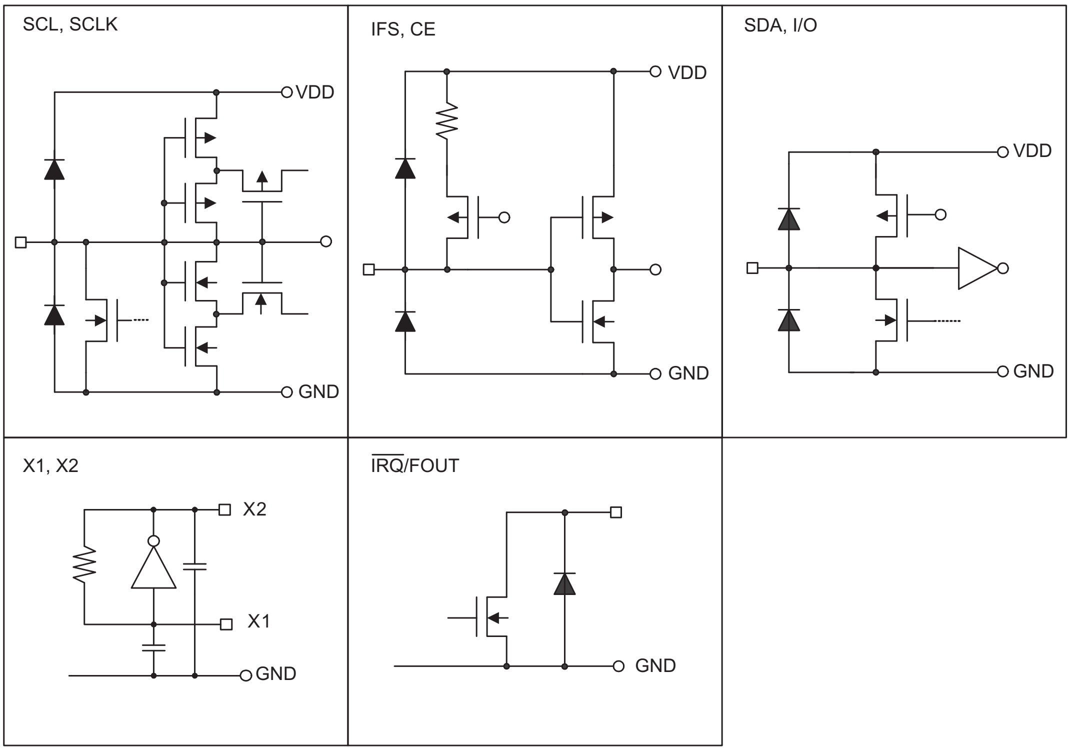
Unit: μm

Pad No.	X	Y	Pad No.	X	Y
1	–520.005	–161.460	6	–520.005	–646.610
2	–520.005	–256.460	7	521.000	–625.000
3	–520.005	–360.130	8	521.000	–530.000
4	–520.005	–455.130	9	521.000	–425.300
5	–520.005	–550.130	10	516.450	–288.400

Pad Description

Pad No.	Pad Name	I/O	Description
1	X1	I	32768Hz crystal input pin
2	X2	O	32768Hz crystal output pin
3	VBAT	—	Battery power supply
4	VSS	—	Negative power supply, ground
5	IFS	I	Interface selection pin. I^2C interface is selected when IFS is unconnected, 3-wire interface is selected when IFS is connected to VSS.
6	CE	I	Chip Enable for 3-wire interface Not used for I^2C interface
7	SDA/I/O	I/O	Serial Data Input/Output for I^2C and 3-wire interfaces
8	SCL/SCLK	I/O	Serial Clock Input for I^2C and 3-wire interfaces
9	IRQ/FOUT	O	Interrupt/Frequency Output, this pin is open drain output
10	VDD	—	Positive power supply

Approximate Internal Connections



Absolute Maximum Ratings

Supply Voltage .... V_{SS}–0.3V to V_{SS}+6.0V
Input Voltage .... V_{SS}–0.3V to V_{DD}+0.3V
Storage Temperature .... –50°C to 125°C
Operating Temperature.. –40°C to 85°C

Note: These are stress ratings only. Stresses exceeding the range specified under "Absolute Maximum Ratings" may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

D.C. Characteristics

Ta=–40°C~85°C

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
V_{DD}	Supply Voltage	—	—	2.7	—	5.5	V
V_{BAT}	Battery Supply Voltage	—	—	2.0	—	5.5	V
I_{STB}	Standby Current	—	V_{BAT}=3V, "CH"=1	—	—	0.1	μA
I_{BAT}	Battery Supply Current	—	V_{BAT}=3V, "CH"=0	—	0.8	1.2	μA
I_{DD1}	Supply Current (Low Power Mode)	3V	SCL/SCLK=0Hz, "LPM"=1	—	5	15	μA
		5V		—	15	30	μA
I_{DD2}	Supply Current	3V	SCL/SCLK=0Hz, "LPM"=0	—	50	100	μA
		5V		—	70	150	μA
I_{DD3}	Supply Current with I^2C Active	3V	SCL=400kHz	—	80	150	μA
		5V		—	150	300	μA
I_{DD4}	Supply Current with 3-Wire Active	3V	SCLK=1MHz	—	100	200	μA
		5V	SCLK=2MHz	—	300	500	μA
V_{IH}	"H" Input Voltage	—	—	$0.7V_{DD}$	—	—	V
V_{IL}	"L" Input Voltage	—	—	—	—	$0.3V_{DD}$	V
V_{OH}	I/O High Level Output Voltage	3V	I_{OH1}= –1.5mA	2.7	—	—	V
		5V	I_{OH1}= –3.0mA	4.5	—	—	V
V_{OL1}	I/O, SCL and SDA Low Level Output Voltage	3V	I_{OL1}= 3.0mA	0	—	0.4	V
		5V	I_{OL1}= 6.0mA	0	—	0.4	V
V_{OL2}	IRQ Low Level Output Voltage	3V	I_{OL2}= 1.5mA	0	—	0.4	V
		5V	I_{OL2}= 3.0mA	0	—	0.4	V
V_{COMP}	V_{BAT} Mode Compared Voltage	—	—	2.40	2.55	2.70	V
	Hysteresis	—	—	—	25	—	mV
V_{BATHYS}	V_{BAT} Hysteresis	—	—	—	40	—	mV

A.C. Characteristics

V_{DD}=2.7V~5.5V, Ta=–40°C~85°C

Power-Down Timing

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
t_{FSR}	VDD Falling Slew Rate	—	—	—	—	10	V/ms

Note: in order to ensure proper timekeeping, the t_{FSR} specification must be followed.

I^2C Interface

Symbol	Parameter	Remark	Min.	Typ.	Max.	Unit
f_{SCL}	Clock frequency	—	—	—	400	kHz
t_{HIGH}	Clock High Time	—	600	—	—	ns
t_{LOW}	Clock Low Time	—	1300	—	—	ns
t_r	SDA and SCL Rise Time	Note	—	—	300	ns
t_f	SDA and SCL Fall Time	Note	—	—	300	ns
$t_{HD:STA}$	START Condition Hold Time	After this period, the first clock pulse is generated.	600	—	—	ns
$t_{SU:STA}$	START Condition Setup Time	Only relevant for repeated START condition.	600	—	—	ns
$t_{HD:DAT}$	Data Input Hold Time	—	0	—	—	ns
$t_{SU:DAT}$	Data Input Setup Time	—	100	—	—	ns
$t_{SU:STO}$	STOP Condition Setup Time	—	600	—	—	ns
t_{AA}	Output Valid from Clock	—	—	—	900	ns
t_{BUF}	Bus Free Time	Time in which the bus must be free before a new transmission can start	1300	—	—	ns
t_{SP}	Input Filter Time Constant (SDA and SCL Pins)	Noise suppression time	—	—	50	ns

Note: These parameters are periodically sampled but not 100% tested

3-wire Interface

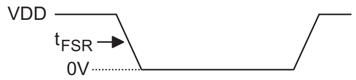
Ta=–40°C~85°C

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
f_{SCLK}	Serial Clock	3V	—	—	—	1	MHz
		5V	—	—	—	2	MHz
t_{DC}	Data to Clock Setup	3V	—	100	—	—	ns
		5V	—	50	—	—	ns
t_{CDH}	Clock to Data Hold	3V	—	140	—	—	ns
		5V	—	70	—	—	ns
t_{CDD}	Clock to Data Delay	3V	—	—	—	400	ns
		5V	—	—	—	200	ns
t_{CL}	Clock Low Time	3V	—	500	—	—	ns
		5V	—	250	—	—	ns
t_{CH}	Clock High Time	3V	—	500	—	—	ns
		5V	—	250	—	—	ns
t_r	Clock Rise and Fall time	3V	—	—	—	1000	ns
t_f		5V	—	—	—	500	ns

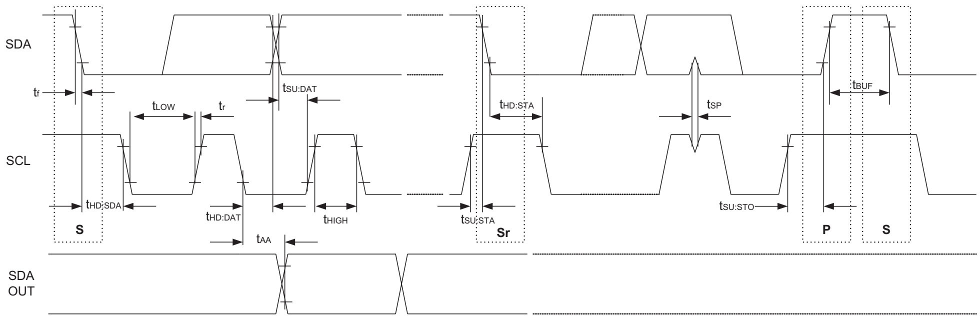
Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
t_{CC}	Reset to Clock Setup	3V	—	2	—	—	μs
		5V	—	1	—	—	μs
t_{CCH}	Clock to Reset Hold	3V	—	120	—	—	ns
		5V	—	60	—	—	ns
t_{CWH}	Reset Inactive Time	3V	—	2	—	—	μs
		5V	—	1	—	—	μs
t_{CDZ}	Reset to I/O High Impedance	3V	—	—	—	140	ns
		5V	—	—	—	70	ns

Timing Diagrams

Power-Down Timing

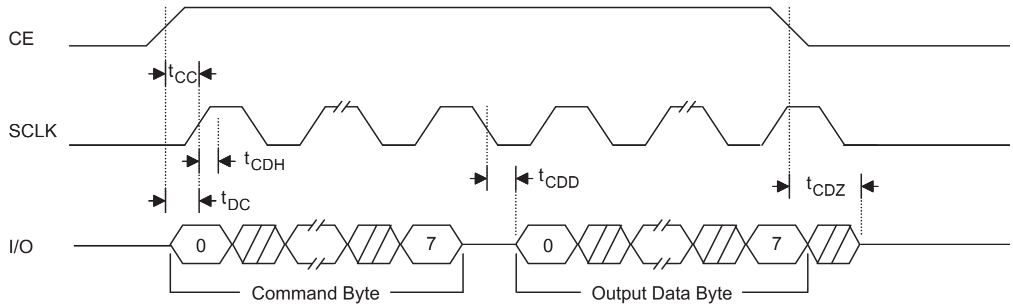


I^2C Interface

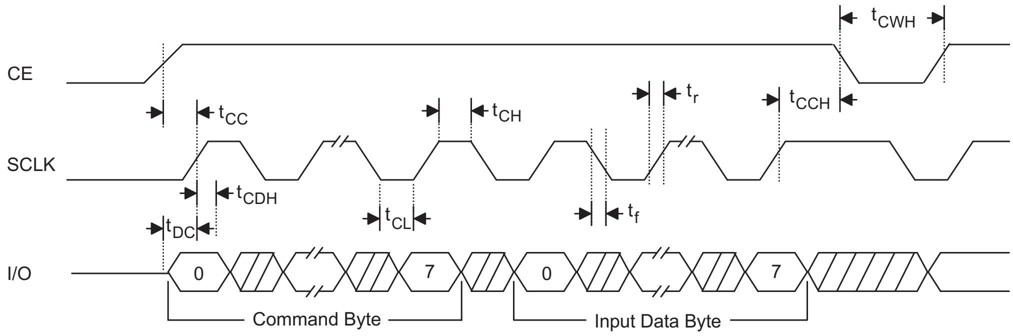


3-wire Interface

Read Data Transfer



Write Data Transfer



Crystal Specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
f_O	Nominal Frequency	—	32.768	—	kHz
ESR	Series Resistance	—	—	50	kΩ
C_L	Load Capacitance	—	12.5	—	pF

Functional Description

The HT1382 is a low power real time clock device which provides full date and time functions. Communication with the device is provided through two integral serial interfaces, I²C or 3-wire. The device version selects the type of interface. The clock and calendar information is generated in BCD format and also has alarm features. The calendar is accurate until the year 2099, with automatic leap year correction.

Basic timing is provided using an external 32768Hz crystal, for which the device includes load capacitances of 12.5pF. An oscillator compensation function is provided to compensate for crystal oscillator temperatures. With fully integrated power control circuitry which can detect power failures, the device can automatically switch to a reserve battery supply when a power failure occurs.

Power Control Function

The internal battery switchover circuit continually monitors the main power supply on the VDD pin and automatically switches to the backup battery supply when a power failure condition is detected.

In the battery backup mode, the interface is disabled to minimise power consumption. The interface inputs will not be recognized which prevents extraneous data being written to the device. The interface outputs are high-impedance. All RTC function are operational when the device is in the battery backup mode.

Normal Mode (V_{DD}) to Battery Backup Mode (V_{BAT})

To switch from the V_{DD} to V_{BAT} Mode , both of the following conditions must be valid:

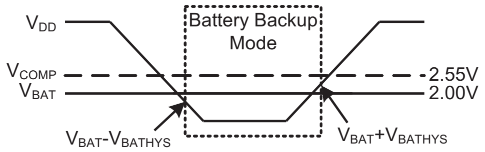
$V_{DD} < V_{BAT}-V_{BATHYS}$ and $V_{DD} < V_{COMP}$

Battery Backup Mode (V_{BAT}) to Normal Mode (V_{DD})

To switch from the V_{BAT} to V_{DD} Mode, one of the following conditions must be valid:

$V_{DD} > V_{BAT} + V_{BATHYS}$ or $V_{DD} > V_{COMP} + V_{COMPHYS}$

The power control situation is illustrated graphically below:



Note: Battery switchover when $V_{BAT} < V_{COMP}$

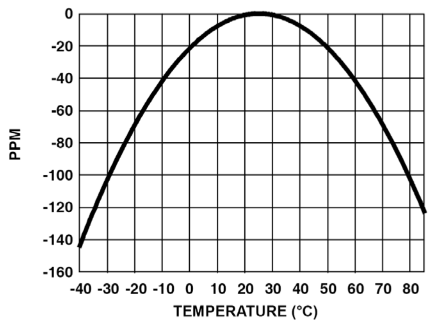
Low Power Mode

In normal mode, the HT1382 switched into battery backup mode when the V_{DD} power is lost. This will ensure that the device can accept a wide range of backup voltages from many types of sources while reliably switching into backup mode. Another mode, called Low Power Mode, is available to allow direct switching from V_{DD} to V_{BAT} without requiring V_{DD} to drop below V_{COMP}. The power switchover circuit is disabled and less power is used while operating from V_{DD}. Low Power Mode is activated via the LPM bit.

Low Power Mode is useful when V_{DD} is normally higher than V_{BAT}. The device will switch from V_{DD} to V_{BAT} when V_{DD} drops below V_{BAT}, with about 40mVof hysteresis to prevent any switchback of V_{DD} after switchover. In a system with V_{DD}=5V and V_{BAT}=3V, Low Power Mode can be used. However, it is not recommended to use Low Power Mode in V_{DD}=3.3V±10%, V_{BAT}≥3V.

Clock Compensation

The device includes a digital trimming method for clock error correction due to temperature variations of the crystal oscillator. This can be implemented as manufacturing calibration or user active calibration. The crystal accuracy to temperature characteristic is similar to that shown in the diagram.



The Digital Trimming Register, DT, is used for clock compensation. Correction is performed once every 10 seconds or 30 seconds. The minimum resolution is 3.052ppm or 1.017ppm and the device has a correction in the range of ±192.276ppm or ±64.071ppm.

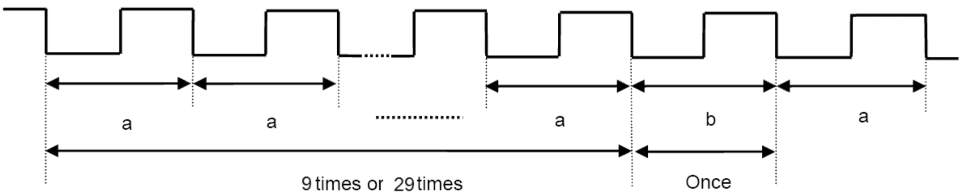
Set FO3~FO0= ″1010″, the FOUT pin will have 1Hz clock pulse output. Measure the FOUT frequency using a high-accuracy frequency counter with 7 or more digits. The correction value is calculated using the formula shown below.

$$\text{Correction value} = \text{integral value}\left(\frac{\text{1Hz - (measured value)}}{\text{minimum resolution (3.052ppm or 1.014ppm)}}\right)$$

When clock compensation is used, set FO3~FO0=″1010″, and the FOUT pin will have 1Hz clock pulse output. The cycle changes once in 10 seconds or in 30 seconds as shown below. In the diagram ″a″ denotes a non-correctional cycle, and ″b″ denotes a correctional cycle. Measure ″a″ and ″b″ using a high-accuracy frequency counter of 7 or more digits. Calculate the average frequency based on the measured result.

For DTS = 0, the average period = (a × 9 + b) ÷ 10

For DTS = 1, the average period = (a × 29 + b) ÷ 30



Register Description

The device includes 16 registers which are used to control functions such as the RTC, Status, Alarm, Frequency output etc. There are also five bytes of EEPROM which contain the clock compensation settings and stored user data. The RTC and Alarm register data is stored in BCD format, while other data is stored in binary format. The register map shows the address definitions for the I²C interface. The command byte and R/W bit are used for the 3-wire interface.

Address	Register Definition								Register Name	Range Data	Default	Bit R/W	Command Byte
	D7	D6	D5	D4	D3	D2	D1	D0					
00H	CH	10 SEC			SEC				Seconds	00~59	80H	W R	10000000 10000001
01H	0	10 MIN			MIN				Minutes	00~59	00H	W R	10000010 10000011
02H	12/ 24	0 0	AP 10	HR HR	HOUR				Hours	01~12 00~23	12H	W R	10000100 10000101
03H	0	0	10 DATE		DATE				Date	01~31	01H	W R	10000110 10000111
04H	0	0	0	10M	MONTH				Month	01~12	01H	W R	10001000 10001001
05H	0	0	0	0	0	DAY			Day	01~07	01H	W R	10001010 10001011
06H	10 YEAR				YEAR				Year	00~99	00H	W R	10001100 10001101
07H	WP	0	0	0	0	0	0	0	ST	—	80H	W R	10001110 10001111
08H	ARE	0	0	EWE	EB	AI	BE	0	ST	—	00H	W R	10010000 10010001
09H	IME	AE	LPM	OEOBM	FO3	FO2	FO1	FO0	INT	—	00H	W R	10010010 10010011
0AH	SECEN	AL. 10SEC			AL. SEC				Seconds Alarm	00~59	00H	W R	10010100 10010101
0BH	MINEN	AL. 10MIN			AL. MIN				Minutes Alarm	00~59	00H	W R	10010110 10010111
0CH	HREN	0	AL. 10HR		AL. HOUR				Hours Alarm	01~12 00~23	00H	W R	10011000 10011001
0DH	DTEN	0	AL. 10DT		AL. DATE				Date Alarm	01~31	00H	W R	10011010 10011011
0EH	MOEN	0	0	AL. 10M	AL. MONTH				Month Alarm	01~12	00H	W R	10011100 10011101
0FH	DAYEN	0	0	0	0	AL. DAY			Day Alarm	01~07	00H	W R	10011110 10011111
EEPROM Data													
10H	DTS	DT6	DT5	DT4	DT3	DT2	DT1	DT0	DT	—	—	W R	10100000 10100001
11H	EEPROM User Data								USR	—	—	W R	10100010 10100011
12H	EEPROM User Data								USR	—	—	W R	10100100 10100101
13H	EEPROM User Data								USR	—	—	W R	10100110 10100111
14H	EEPROM User Data								USR	—	—	W R	10101000 10101001

Real Time Clock Register

The RTC register stores the Year, Day, Month, Date, Hours, Minutes and, Second data in BCD format.

12/24 Hour Mode

Bit D7 of the hour register is defined as the 12-hour or 24-hours mode select bit. If the bit is ″1″, the RTC uses a 24-hour format. If ″0″, the RTC uses a 12-hour format. The default value is ″0″.

AM/PM Mode

There are two function for the D5 bit in the hour register which is determined by the D7 bit. In the 12-hour mode the bit is used for AM/PM selection. When D5 is ″1″, it will be PM, otherwise it will be AM. In the 24-hour mode, the bit is used to set the second 10-hour bit(20~23 hours).

Leap Years

Leap years add an extra day for February 29 and are defined as those years that are divisible by 4. The device will provide automatic correction for leap years until year 2099.

Clock HALT Bit – CH

This bit enables/disables the oscillator. The CH bit is set high to disable the oscillator and cleared to zero is enable it. The default value is define as ″1″.

Write Protect Bit – WP

The WP bit is set high to prevent data writes and cleared to zero to allow data to be written. The default value is define as ″1″.

Battery Enable Bit – BE

When the device enters the battery backup mode, the BE bit is set to ″1″. This bit can be cleared to ″0″ either manually by the user or automatically reset by the ARE pin. Only a ″0″ an be written to this bit, not a ″1″.

Alarm Interrupt Bit – AI

When the RTC register values match the alarm register values, the AI bit will be set to ″1″. This bit can be reset to ″0″ either manually by the user or automatically reset by the ARE pin. Only a ″0″ an be written to this bit, not a ″1″. The AI bit will be set by an alarm occurring during a read operation ad will remain set until after the read operation is complete.

Auto Reset Enable Bit – ARE

This bit enables/disables the automatic reset of the BE and AI status bits only. When ARE is set to ″1″, BE and AI will be reset to ″0″ after reading these registers. When ARE is cleared to ″0″, the user must manually reset the BE and AI bits.

EEPROM Write Enable Bit – EWE

When EWE is cleared to ″0″, the EEPROM is read only, and the user can not write data to the EEPROM. When EWE is set to ″1″, the user can write data to the EEPROM. Before writing data to the EEPROM, this bit must be set to ″1″.

EEPROM Busy Status Bit – EB

This bit is set to ″1″ when a write operation to the EEPROM has not completed. When this bit is set to ″1″, reading data from the EEPROM or writing data to the EEPROM is invalid. After an EEPROM write has finished, this bit will be cleared to ″0″ and the user can read data from the EEPROM or write data to the EEPROM.

Output Enable On Battery Mode Bit – OEOBM

This bit enables/disables the $\overline{\text{IRQ}}$/FOUT pin in the battery mode. When the OEOBM bit is set to ″1″, the $\overline{\text{IRQ}}$/FOUT pin is disabled in the battery mode and the frequency output and alarm function are disabled. When the OEOBM bit is cleared to ″0″, the $\overline{\text{IRQ}}$/FOUT pin is enabled in the battery mode.

Low Power Mode Bit – LPM

This bit enables/disables the Low Power Mode. When the LPM bit is cleared to ″0″, the device will be in the normal mode and will use the V_{BAT} supply when $V_{DD} < V_{BAT}$ and $V_{DD} < V_{COMP}$. When the LPM bit is set to ″1″, the device is in the Low Power Mode and uses the V_{BAT} supply when $V_{DD} < V_{BAT}$.

Frequency Output Bits – FO3~FO0

These bits enable/disable the frequency output function and selects the output frequency at the FOUT pin. The frequency selection table is shown below. It overrides the alarm mode. The 1, 1/2, 1/4, 1/8, 1/16, 1/32 frequency outputs are compensated.

FOUT(Hz)	FO3	FO2	FO1	FO0
—	0	0	0	0
32768	0	0	0	1
4096	0	0	1	0
1024	0	0	1	1
64	0	1	0	0
32	0	1	0	1
16	0	1	1	0
8	0	1	1	1
4	1	0	0	0
2	1	0	0	1
1	1	0	1	0
1/2	1	0	1	1
1/4	1	1	0	0
1/8	1	1	0	1
1/16	1	1	1	0
1/32	1	1	1	1

Alarm Enable Bit – AE

This bit enables/disables the alarm function. When the AE bit is set to ″1″, the alarm function is enabled. When the AE bit is cleared to ″0″, the alarm function is disabled.

Digital Trimming Setting Bits – DTS

This bit sets the digital trimming resolution and adjustment time. The user must detect the status of the EB bit before reading data or writing data. If the EB bit is ″0″, it is valid to read data or write data. If the EB bit is ″1″, it is invalid to read data or write data.

	DTS=″0″	DTS=″1″
Adjustment time	Every 10 seconds	Every 30 seconds
Minimum resolution	3.052ppm	1.017ppm
Correction range	-192.276ppm to +192.276ppm	-64.071ppm to + 64.071ppm

Digital Trimming Bits – DT6~DT0

This digital trimming bit, DT6, is the sign bit. A ″0″ indicates positive calibration and a ″1″ indicates negative calibration. DT5~DT0 are the calibration values and the adjustable range is -63 ~ +63. If DTS is cleared to ″0″, the correction range is -192.276ppm to +192.276ppm and if DTS is set to ″1″, the correction range is -64.071ppm to +64.071ppm. The user must detect the status of EB bit before reading data or writing data. If the EB bit is ″0″, it is valid to read data or write data. If the EB bit is ″1″, it is invalid to read data or write data.

DT6	DT5	DT4	DT3	DT2	DT1	DT0	Value	Correction Value (ppm)	
								DTS=″0″	DTS=″1″
0	1	1	1	1	1	1	+63	+192.276	+64.071
0	1	1	1	1	1	0	+62	+189.224	+63.054
0	1	1	1	1	0	1	+61	+186.172	+62.037
0	1	1	1	1	0	0	+6	+183.120	+61.020
:								:	:
0	01	0	0	0	1	1	+3	+9.156	+3.051
0	0	0	0	0	1	0	+2	+6.104	+2.034
0	0	0	0	0	0	1	+1	+3.052	+1.017
0	0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	1	-1	-3.052	-1.07
1	0	0	0	0	1	0	-2	-6.104	-2.034
1	0	0	0	0	1	1	-3	-9.156	-3.051
:								:	:
1	1	1	1	1	0	0	-60	-183.120	-61.020
1	1	1	1	1	0	1	-61	-186.172	-62.037
1	1	1	1	1	1	0	-62	-189.224	-63.054
1	1	1	1	1	1	1	-63	-192.276	-64.071

Interrupt Mode Enable Bit – IME

This bit enables/disables the interrupt mode of the alarm function. When the IME bit is set to ″1″, the interrupt mode is enabled and when the IME bit is cleared to ″0″, the interrupt mode is disabled and the alarm operates in single mode.

Alarm Register

The addresses of alarm registers are 0Bh to 10h. The data is stored in the BCD format. The MSB of each alarm register is an enable bit. (enable=″1″). These enable bits specify which alarm registers are used to make the comparison between the alarm registers and the RTC registers. There is no alarm byte for year. When a compare match condition exists, the AI bit is set to ″1″, and the $\overline{\text{IRQ}}$ pin is activated.

To clear an alarm, the AI bit must be cleared to ″0″. If the ARE bit is set to ″1″, the AI bit will automatically be cleared when the status register is read.

There are two alarm operation modes: Single mode and Interrupt Mode.

Single mode: set the AE bit to ″1″, the IME bit to ″0″, and disable the frequency output. When the RTC register values match the alarm registers values, the AI bit will be set to ″1″ and the alarm condition activates the $\overline{\text{IRQ}}$ pin. The $\overline{\text{IRQ}}$ pin will remain low until the AI bit is cleared to ″0″.

Interrupt mode: set the AE bit to ″1″, the IME bit to ″1″, and disable the frequency output. When the RTC registers values match the alarm registers values, the $\overline{\text{IRQ}}$ pin will be pulled low for 250ms and the AI bit will be set to ″1″. This mode allows for a repetitive or recurring alarm function. When the alarm is set, the device will continue to activate an alarm for each match of the alarm and the present time. For example, if only the seconds are set, it will activate an alarm every minute, if only the minutes are set, it will activate an alarm every hour.

EEPROM User Data

The HT1382 provides 4 bytes EEPROM for user. The EEPROM will continue to operate in battery backup mode. However, it should be noted that the I²C/3-wire interface is disabled in battery backup mode. User must detect the status of EB bit before reading data or writing data. If the EB bit is ″0″, it is valid to read data or write data. If the EB bit is ″1″, it is invalid to read data or write data.

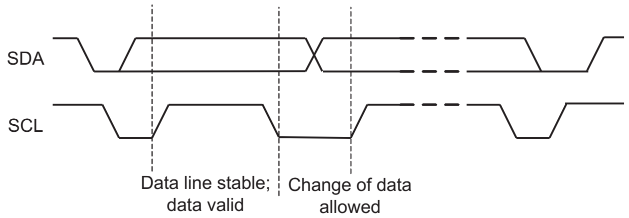
I^2C Serial Interface

The HT1382 includes an I^2C serial interface. The I^2C bus is used for bidirectional, two-line communication between multiple I^2C devices. The two lines of the interface are the serial data line (SDA) and the serial clock line (SCL).Both lines are connected to the positive supply via a pull-up resistor externally.

When the bus is free, both lines will be high. The output stages of the devices connected to the bus must have open-drain or open-collector output types to implement the wired-AND function necessary for connection. Data transfer is initiated only when the bus is not busy.

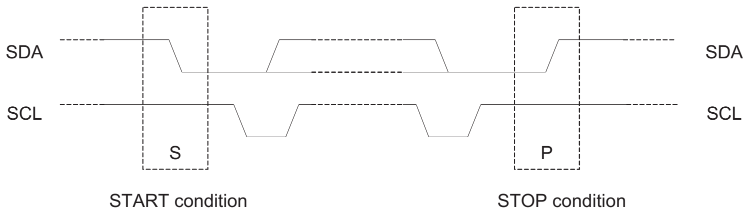
Data Validity

The data on the SDA line must be stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW.



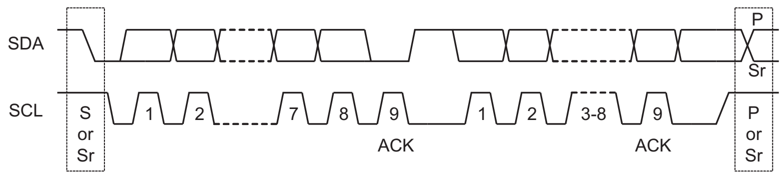
START and STOP Conditions

A HIGH to LOW transition on the SDA line while SCL is HIGH defines a START condition. A LOW to HIGH transition on the SDA line while SCL is HIGH defines a STOP condition. START and STOP conditions are always generated by the master. The bus is considered to be busy after the START condition. The bus is considered to be free again a certain time after the STOP condition. The bus stays busy if a repeated START(Sr) is generated instead of a STOP condition. In this respect, a START(S) and repeated START(Sr) conditions are functionally identical.



Byte Format

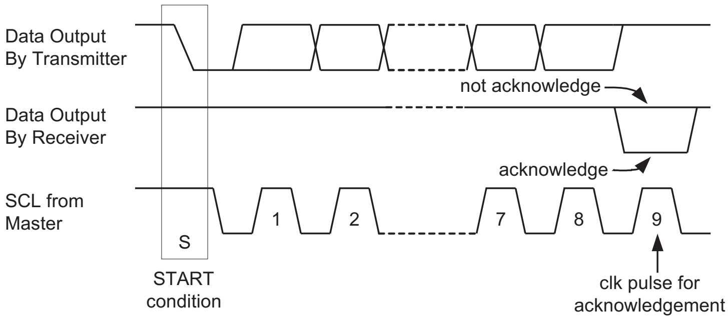
Every byte put on the SDA line must be 8-bits long. The number of bytes that can be transmitted per transfer is unrestricted. Each byte has to be followed by an acknowledge bit. Data is transferred with the most significant bit (MSB) first.



Acknowledge

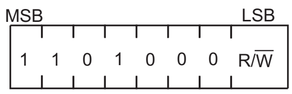
Each bytes of eight bits is followed by one acknowledge bit. This acknowledge bit is a low level placed on the bus by the receiver. The master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge (ACK) after the reception of each byte.

The acknowledging device must first pull down the SDA line during the acknowledge clock pulse so that it remains LOW during the HIGH period of this clock pulse. A master receiver must signal an end of data to the slave by generating a not-acknowledge (NACK) bit on the last byte that has been clocked out of the slave. In this case, the master receiver must leave the data line HIGH during the 9th pulse to not acknowledge. The master will generate a STOP or repeated START condition.



Device Addressing

The slave address byte is the first byte received following the START condition from the master device. The first seven bits of the first byte make up the slave address. The eighth bit defines a read or write operation to be performed. When this R/$\overline{W}$ bit is ″1″, then a read operation is selected. A ″0″ selects a write operation. The device address bits are ″1101000″. When an address byte is sent, the device compares the first seven bits after the START condition. If they match, the device outputs an acknowledge on the SDA line.

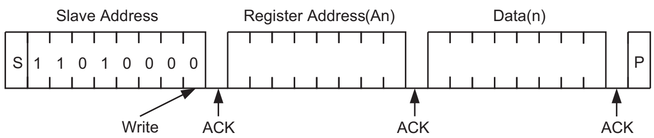


The first byte after the START.

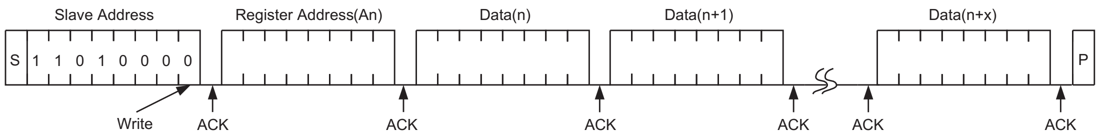
Write Operation

- Byte Write Operation
  A byte write operation requires a START condition, a slave address with R/ bit, a valid Register Address, the required Data and a STOP condition. After each of the three byte transfers, the device responds with an ACK.

- Page Write Operation
  Following a START condition and slave address, a R/ bit is placed on the bus which indicates to the addressed device that a Register Address will follow which is to be written to the address pointer. The data to be written to the memory follows next and the internal address pointer is incremented to the next address location on the reception of an acknowledge clock. After reaching memory location 0Fh, the pointer will be reset to 00h.



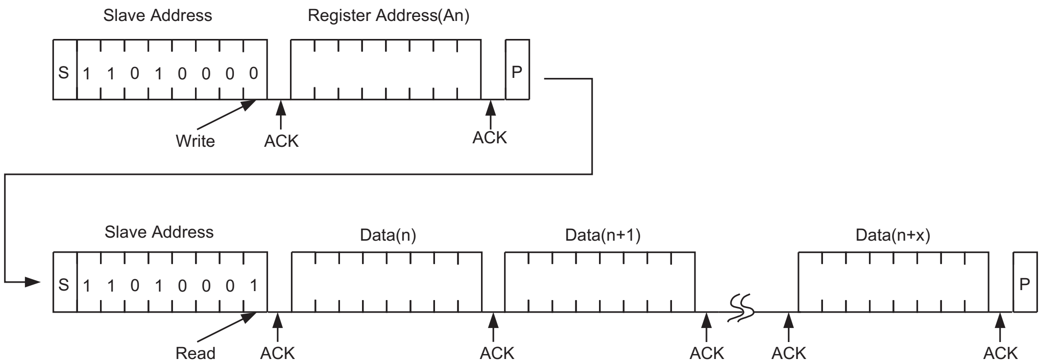
Byte Write Sequence



Page Write Sequence

Read Operation

In this mode, the master reads the device data after setting the slave address. Following the R/$\overline{W}$ bit (="0") and the acknowledge bit, the register address (An) is written to the address $\overline{W}$ pointer. Next the START condition and slave address are repeated followed by the R/$\overline{W}$ bit (="1"). The data which was addressed is then transmitted. The address pointer is only incremented on reception of an acknowledge clock. The device will then place the data at address An+1 on the bus. The master reads and acknowledges the new byte and the address pointer is incremented to "An+2". After reaching the memory location 0Fh, the pointer will be reset to 00h. This cycle of reading consecutive addresses will continue until the master sends a STOP condition.



Read Sequence

3-wire Serial Interface

The device also support a 3-wire serial interface. The CE pin is used to identify the transmitted data. The transmission is controlled by the active HIGH signal CE. Each data transfer is a byte, with the LSB sent first. The first byte transmitted is the Command Byte.

Command Byte

For each data transfer, a Command Byte is initiated to specify which register is accessed. This is to determine whether a read or write cycle is operational and whether a single byte or burst mode transfer is to occur.

R/$\overline{W}$ Signal

The LSB of the Command Byte determines whether the data in the register is to be read or be written to. If it is "0" then this means that it is a write cycle. If it is "1" then this means that it is a read cycle.

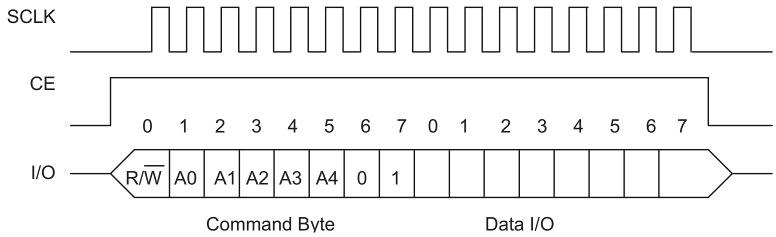
Burst Mode

When the Command Byte is 10111110 or 10111111, the device is configured in the burst mode. In this mode, the address of registers from 00h to 0Fh can be written or read in series, starting with bit 0 of register address 0.

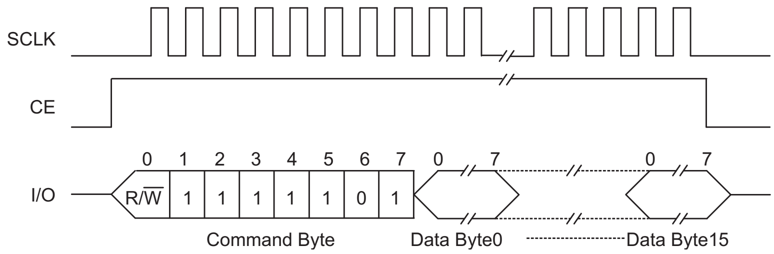
Data Input and Data Out

In writing a data byte, R/$\overline{W}$ is cleared to ″0″ in the Command Byte and is then followed by the corresponding data register address on the rising edge of the next eight SCLK. Additional SCLK cycles are ignored. Data inputs are entered starting with bit 0. In reading data from the register, the R/$\overline{W}$ is set to ″1″ in the Command Byte. The data bits are output on the falling edge of the next eight SCLK cycles. Note that the first data bit to be transmitted on the first falling edge after the last bit of the read command byte is written. Additional SCLK cycles re-transmits the data bytes as long as CE remains at high level. Data outputs are read starting with bit 0.

- Single Byte Transfer

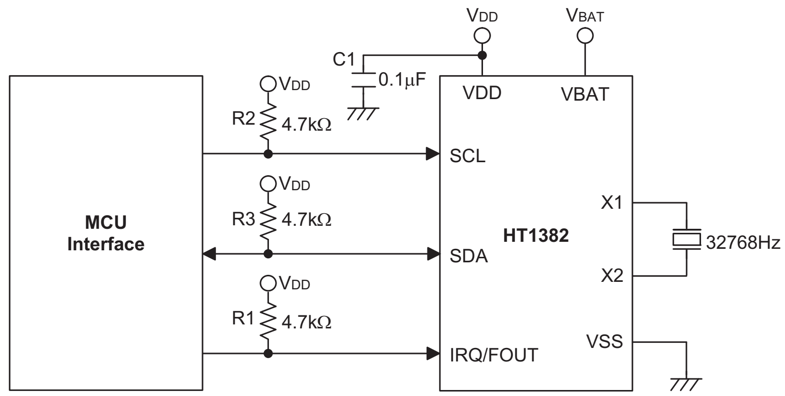


- Burst Mode Transfer

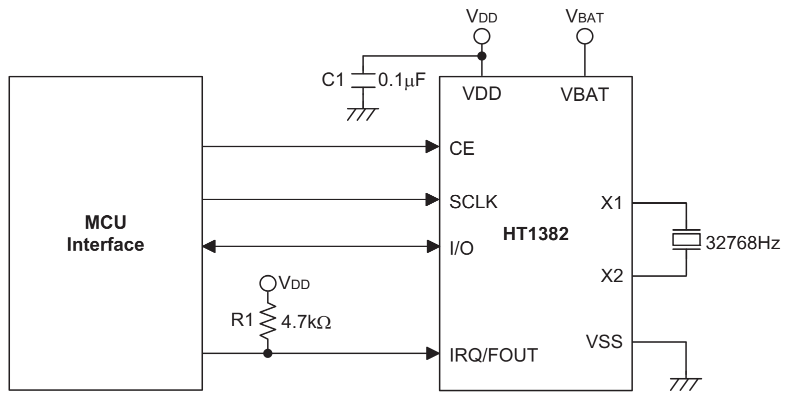


Application Circuits

I²C Serial Interface

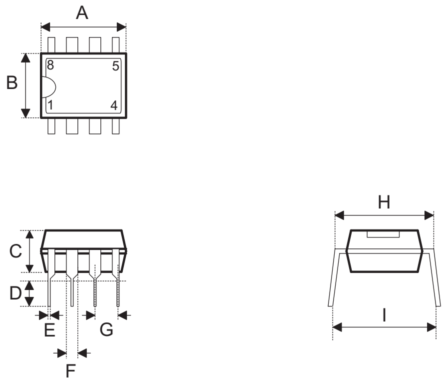


3-wire Serial Interface



Package Information

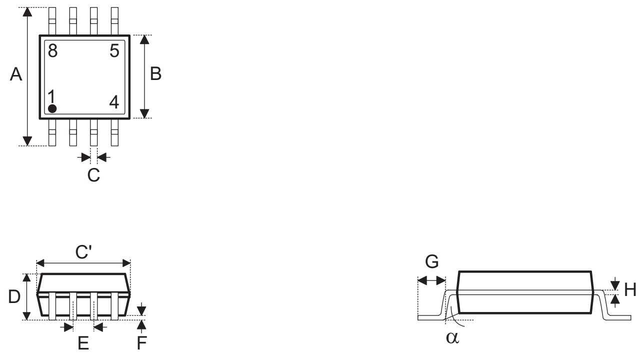
8-pin DIP (300mil) Outline Dimensions



Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A	0.355	—	0.375
B	0.240	—	0.260
C	0.125	—	0.135
D	0.125	—	0.145
E	0.016	—	0.020
F	0.050	—	0.070
G	—	0.100	—
H	0.295	—	0.315
I	—	0.375	—

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	9.02	—	9.53
B	6.10	—	6.60
C	3.18	—	3.43
D	3.18	—	3.68
E	0.41	—	0.51
F	1.27	—	1.78
G	—	2.54	—
H	7.49	—	8.00
I	—	9.53	—

8-pin SOP (150mil) Outline Dimensions

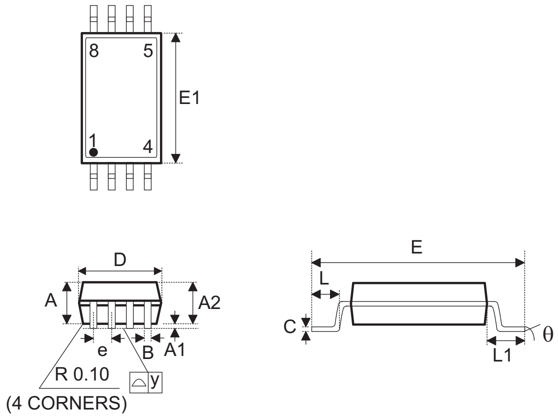


MS-012

Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A	0.228	—	0.244
B	0.150	—	0.157
C	0.012	—	0.020
C′	0.188	—	0.197
D	—	—	0.069
E	—	0.050	—
F	0.004	—	0.010
G	0.016	—	0.050
H	0.007	—	0.010
α	0°	—	8°

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	5.79	—	6.20
B	3.81	—	3.99
C	0.30	—	0.51
C′	4.78	—	5.00
D	—	—	1.75
E	—	1.27	—
F	0.10	—	0.25
G	0.41	—	1.27
H	0.18	—	0.25
α	0°	—	8°

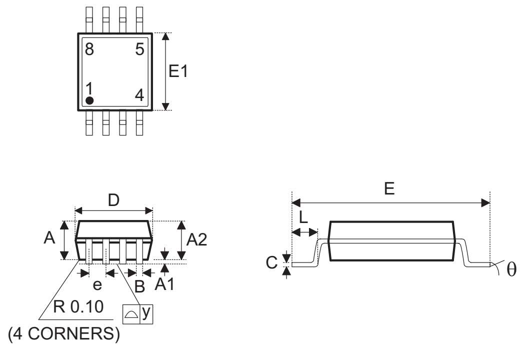
8-pin TSSOP Outline Dimensions



Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A	0.041	—	0.047
A1	0.002	—	0.006
A2	0.031	—	0.041
B	—	0.010	—
C	0.004	—	0.006
D	0.114	—	0.122
E	0.244	—	0.260
E1	0.169	—	0.177
e	—	0.026	—
L	0.020	—	0.028
L1	0.035	—	0.043
y	—	—	0.004
θ	0°	—	8°

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	1.05	—	1.20
A1	0.05	—	0.15
A2	0.80	—	1.05
B	—	0.25	—
C	0.11	—	0.15
D	2.90	—	3.10
E	6.20	—	6.60
E1	4.30	—	4.50
e	—	0.65	—
L	0.50	—	0.70
L1	0.90	—	1.10
y	—	—	0.10
θ	0°	—	8°

8-pin MSOP Outline Dimensions

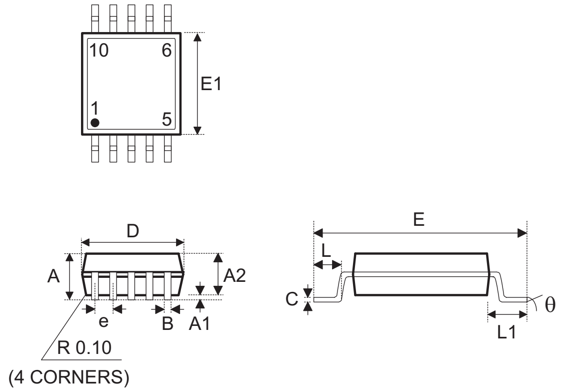


MO-187

Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A	—	—	0.043
A1	0.000	—	0.006
A2	0.030	—	0.037
B	0.009	—	0.013
C	0.003	—	0.009
D	—	0.012	—
E	—	0.193	—
E1	—	0.118	—
e	—	0.026	—
L	0.016	—	0.031
L1	—	0.037	—
y	—	—	0.004
θ	0°	—	8°

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	—	—	1.10
A1	0.00	—	0.15
A2	0.75	—	0.95
B	0.22	—	0.33
C	0.08	—	0.23
D	—	3.00	—
E	—	4.90	—
E1	—	3.00	—
e	—	0.65	—
L	0.40	—	0.80
L1	—	0.95	—
y	—	—	0.10
θ	0°	—	8°

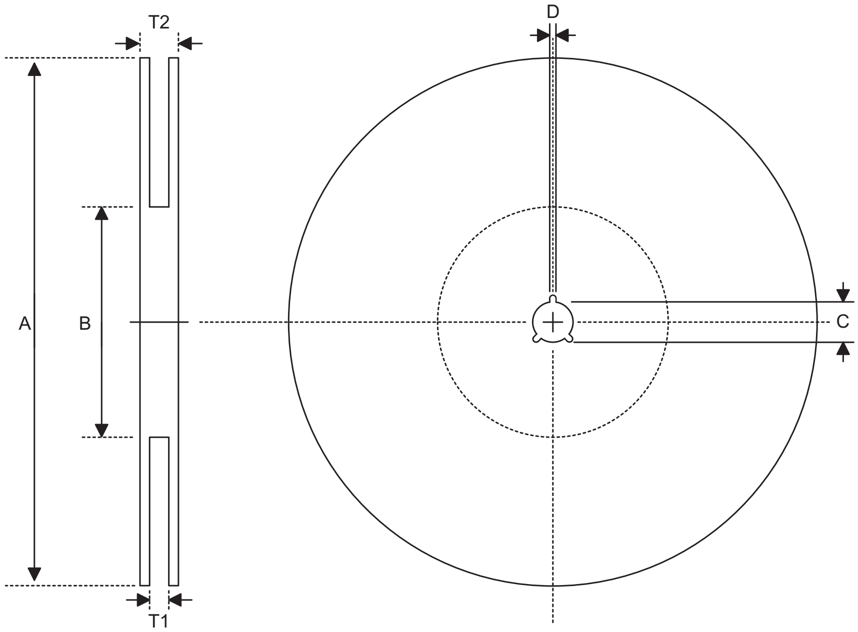
10-pin MSOP Outline Dimensions



Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A	—	—	0.043
A1	0.000	—	0.006
A2	0.030	0.033	0.037
B	0.007	—	0.011
C	—	—	0.010
D	—	0.012	—
E	—	0.193	—
E1	—	0.118	—
e	—	0.020	—
L	0.016	0.024	0.031
L1	—	0.037	—
θ	0°	—	8°

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	—	—	1.10
A1	0.00	—	0.15
A2	0.75	0.85	0.95
B	0.17	—	0.27
C	—	—	0.25
D	—	3.00	—
E	—	4.90	—
E1	—	3.00	—
e	—	0.50	—
L	0.40	0.60	0.80
L1	—	0.95	—
θ	0°	—	8°

Reel Dimensions



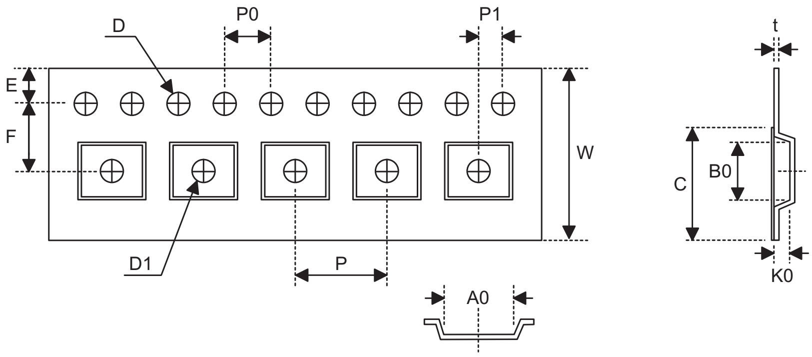
SOP 8N

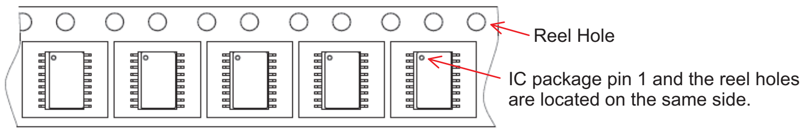
Symbol	Description	Dimensions in mm
A	Reel Outer Diameter	330.0±1.0
B	Reel Inner Diameter	100.0±1.5
C	Spindle Hole Diameter	$13.0^{+0.5/-0.2}$
D	Key Slit Width	2.0±0.5
T1	Space Between Flange	$12.8^{+0.3/-0.2}$
T2	Reel Thickness	18.2±0.2

TSSOP 8L

Symbol	Description	Dimensions in mm
A	Reel Outer Diameter	330.0±1.0
B	Reel Inner Diameter	100.0±1.5
C	Spindle Hole Diameter	$13.0^{+0.5/-0.2}$
D	Key Slit Width	2.0±0.5
T1	Space Between Flange	$12.8^{+0.3/-0.2}$
T2	Reel Thickness	18.2±0.2

Carrier Tape Dimensions





SOP 8N

Symbol	Description	Dimensions in mm
W	Carrier Tape Width	12.0 $^{+0.3/-0.1}$
P	Cavity Pitch	8.0±0.1
E	Perforation Position	1.75±0.1
F	Cavity to Perforation (Width Direction)	5.5±0.1
D	Perforation Diameter	1.55±0.1
D1	Cavity Hole Diameter	1.50 $^{+0.25/-0.00}$
P0	Perforation Pitch	4.0±0.1
P1	Cavity to Perforation (Length Direction)	2.0±0.1
A0	Cavity Length	6.4±0.1
B0	Cavity Width	5.2±0.1
K0	Cavity Depth	2.1±0.1
t	Carrier Tape Thickness	0.30±0.05
C	Cover Tape Width	9.3±0.1

TSSOP 8L

Symbol	Description	Dimensions in mm
W	Carrier Tape Width	$12.0^{+0.3/-0.1}$
P	Cavity Pitch	8.0±0.1
E	Perforation Position	1.75±0.10
F	Cavity to Perforation (Width Direction)	5.5±0.5
D	Perforation Diameter	$1.5^{+0.1/-0.0}$
D1	Cavity Hole Diameter	$1.5^{+0.1/-0.0}$
P0	Perforation Pitch	4.0±0.1
P1	Cavity to Perforation (Length Direction)	2.0±0.1
A0	Cavity Length	7.0±0.1
B0	Cavity Width	3.6±0.1
K0	Cavity Depth	1.6±0.1
t	Carrier Tape Thickness	0.300±0.013
C	Cover Tape Width	9.3±0.1

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