### Features

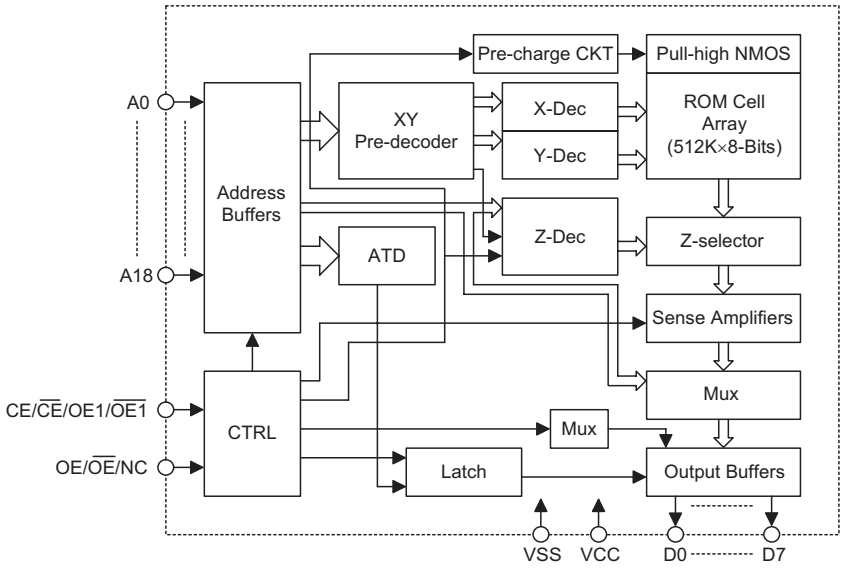
- Operating voltage: 2.7V~5.5V
- Low power consumption
  - Operation: 25mA max. ($V_{CC}$=5V)
    10mA max. ($V_{CC}$=3V)
  - Standby: 30μA max. ($V_{CC}$=5V)
    10μA max. ($V_{CC}$=3V)
- Access time: 120ns max. ($V_{CC}$=5V)
  250ns max. ($V_{CC}$=3V)
- 524288×8-bit of mask ROM
- Mask option: chip enable CE/$\overline{CE}$/OE1/$\overline{OE1}$, and output enable OE/$\overline{OE}$/NC
- TTL compatible inputs and outputs
- Tristate outputs
- Fully static operation
- 32-pin DIP/SOP/PLCC package

### General Description

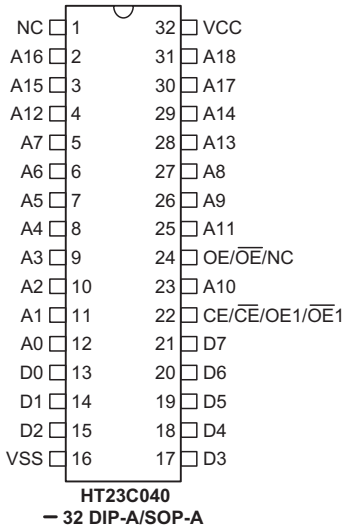
The HT23C040 is a read-only memory with high performance CMOS storage device whose 4096K of memory is arranged into 524288 word by 8 bits.

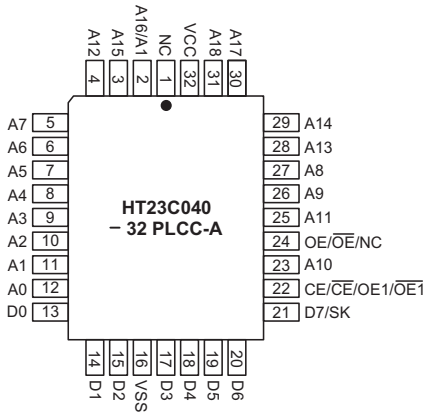
For application flexibility, the chip enable and output enable control pins can be selected as active high or active low. This flexibility not only allows easy interface with most microprocessors, but also eliminates bus contention in multiple bus microprocessor systems. An additional feature of the HT23C040 is its ability to enter the standby mode whenever the chip enable (CE/$\overline{CE}$) is inactive, thus reducing current consumption to below 30μA. The combination of these functions makes the chip suitable for high density low power memory applications.

### Block Diagram



## Pin Assignment




## Pin Description

| Pin Name | I/O | Description |
|---|---|---|
| NC | — | No connection |
| A0~A18 | I | Address inputs |
| D0~D7 | O | Data outputs |
| VSS | — | Negative power supply, ground |
| CE/$\overline{CE}$/OE1/$\overline{OE1}$ | I | Chip enable/Output enable input |
| OE/$\overline{OE}$/NC | I | Output enable input |
| VCC | — | Positive power supply |

## Absolute Maximum Ratings

Supply Voltage.....$V_{SS}$–0.3V to $V_{CC}$+6V

Input Voltage.....$V_{SS}$–0.3V to $V_{CC}$+0.3V

Storage Temperature.....–50°C to 125°C

Operating Temperature.....–40°C to 85°C

Note: These are stress ratings only. Stresses exceeding the range specified under "Absolute Maximum Ratings" may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

## D.C. Characteristics

$T_a$=–40°C to 85°C

| Symbol | Parameter | Test Conditions | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| | | $V_{CC}$ | Conditions | | | | |
| **Supply Voltage: 4.5V~5.5V** | | | | | | | |
| $V_{CC}$ | Operating Voltage | — | — | 4.5 | — | 5.5 | V |
| $I_{CC1}$ | Operating Current | 5V | O/P No load, f=5MHz | — | — | 25 | mA |
| $V_{IL1}$ | Input Low Voltage | 5V | — | $V_{SS}$ | — | 0.8 | V |
| $V_{IH1}$ | Input High Voltage | 5V | — | 2.2 | — | $V_{CC}$ | V |
| $V_{OL1}$ | Output Low Voltage | 5V | $I_{OL}$=3.2mA | — | — | 0.4 | V |
| $V_{OH1}$ | Output High Voltage | 5V | $I_{OH}$=–1mA | 2.4 | — | $V_{CC}$ | V |
| $I_{LI}$ | Input Leakage Current | 5V | $V_{IN}$=0 to $V_{CC}$ | — | — | 10 | μA |
| $I_{LO}$ | Output Leakage Current | 5V | $V_{OUT}$=0 to $V_{CC}$ | — | — | 10 | μA |
| $I_{STB1}$ | Standby Current | 5V | CE=$V_{IL}$, $\overline{CE}$=$V_{IH}$ | — | — | 1.5 | mA |
| $I_{STB2}$ | Standby Current | 5V | $\overline{CE}\leq 0.2V$<br>$\overline{CE}\geq V_{CC}-0.2V$ | — | — | 30 | μA |
| $C_{IN}$ | Input Capacitance (See note) | — | f=1MHz | — | — | 10 | pF |
| $C_{OUT}$ | Output Capacitance (See note) | — | f=1MHz | — | — | 10 | pF |
| **Supply Voltage: 2.7V~3.3V** | | | | | | | |
| $V_{CC}$ | Operating Voltage | — | — | 2.7 | — | 3.3 | V |
| $I_{CC2}$ | Operating Current | 3V | O/P No load, f=5MHz | — | — | 10 | mA |
| $V_{IL2}$ | Input Low Voltage | 3V | — | $V_{SS}$ | — | 0.4 | V |
| $V_{IH2}$ | Input High Voltage | 3V | — | 1.5 | — | $V_{CC}$ | V |
| $V_{OL2}$ | Output Low Voltage | 3V | $I_{OL}$=2mA | — | — | 0.4 | V |
| $V_{OH2}$ | Output High Voltage | 3V | $I_{OH}$=–0.6mA | 1.5 | — | $V_{CC}$ | V |
| $I_{LI}$ | Input Leakage Current | 3V | $V_{IN}$=0 to $V_{CC}$ | — | — | 10 | μA |
| $I_{LO}$ | Output Leakage Current | 3V | $V_{OUT}$=0 to $V_{CC}$ | — | — | 10 | μA |
| $C_{IN}$ | Input Capacitance (See Note) | — | f=1MHz | — | — | 10 | pF |
| $C_{OUT}$ | Output Capacitance (See Note) | — | f=1MHz | — | — | 10 | pF |

Note: These parameters are periodically sampled but not 100% tested.

## A.C. Characteristics

$T_a$=–40°C to 85°C

| Symbol | Parameter | 3V±10% | | 5V±10% | | Unit |
|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | |
| $t_{CYC}$ | Cycle Time | 200 | — | 120 | — | ns |
| $t_{AA}$ | Address Access Time | — | 250 | — | 120 | ns |
| $t_{ACE}$ | Chip Enable Access Time | — | 250 | — | 120 | ns |
| $t_{AOE}$ | Output Enable Access Time | — | 150 | — | 80 | ns |
| $t_{OH}$ | Output Hold Time | — | — | 10 | — | ns |
| $t_{OD}$ | Output Disable Time (See Note) | — | — | — | 70 | ns |
| $t_{OE}$ | Output Enable Time (See Note) | — | — | 10 | — | ns |

Note: These parameters are periodically sampled but not 100% tested.

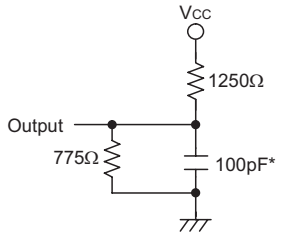
**A.C. Test Condition**

Output load: see figure right

Input rise and fall time: 10ns

Input pulse levels: 0.4V to 2.4V

Input and output timing reference levels:
0.8V and 2.0V ($V_{CC}$=5V)
1.5V ($V_{CC}$=3V)




* Including scope and jig

**Output Load Circuit**

## Functional Description

The HT23C040 has two modes, namely data read mode and standby mode, controlled by CE/$\overline{CE}$/OE1/$\overline{OE1}$ and OE/$\overline{OE}$/NC inputs.

- Standby mode
  The HT23C040 offers lower current consumption, controlled by the chip enable input (CE/$\overline{CE}$). When a low/high level is applied to the CE/$\overline{CE}$ input regardless of the output enable (OE/$\overline{OE}$/NC) states the chip will enter the standby mode.

- Data read mode
  When both the chip enable (CE/$\overline{CE}$/OE1/$\overline{OE1}$) and the output enable (OE/$\overline{OE}$/NC) are active, the chip is in data read mode. Otherwise, active CE/$\overline{CE}$ and inactive OE/$\overline{OE}$/NC result in deselect mode. The output will remain in Hi-Z state.

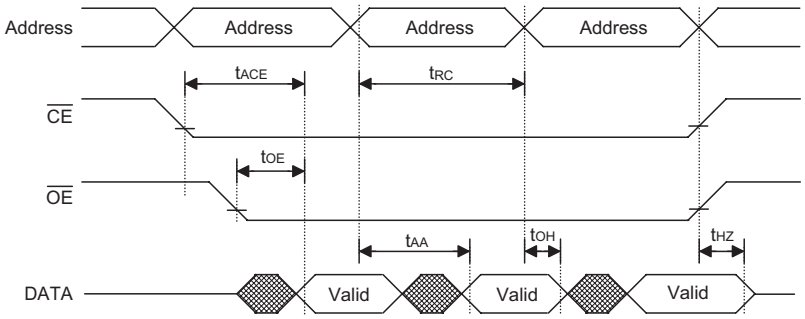
**Operation Truth Table**

| Mode | CE/$\overline{CE}$ | OE/$\overline{OE}$ | A0~A18 | D0~D7 |
|---|---|---|---|---|
| Read | H/L | H/L | Valid | Data Out |
| Deselect | H/L | L/H | X | High Z |
| Standby | L/H | X | X | High Z |

Note: H=$V_{IH}$, L=$V_{IL}$, X=$V_{IH}$ or $V_{IL}$

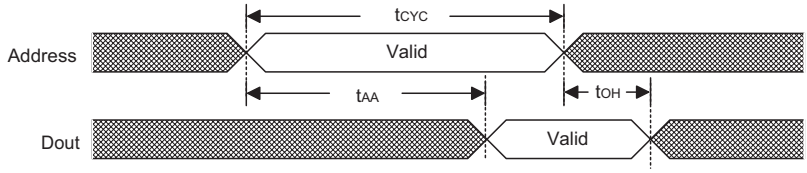
## Timing Diagrams

**Random Read**

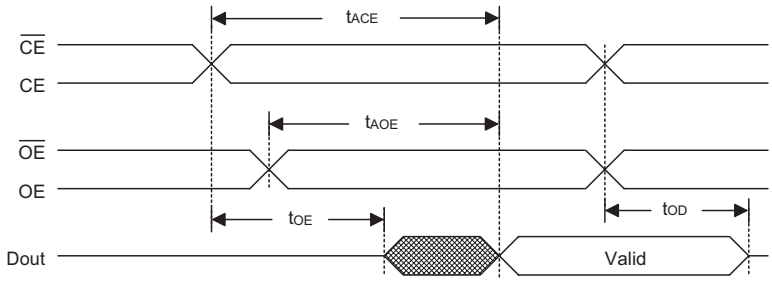



Note: $\overline{CE}$, $\overline{OE}$ are enable

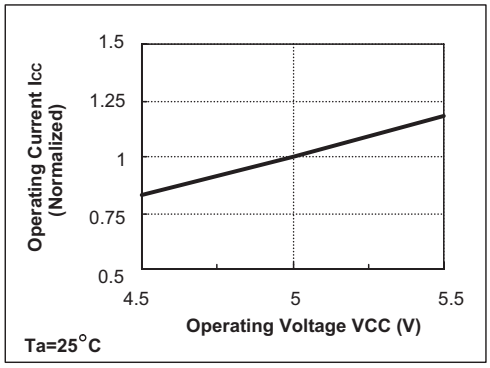
**Propagation Delay Due to Address (CE/$\overline{CE}$/OE1/$\overline{OE1}$ and OE/$\overline{OE}$ are Active)**

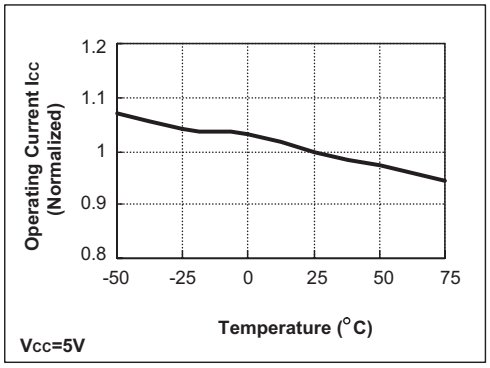


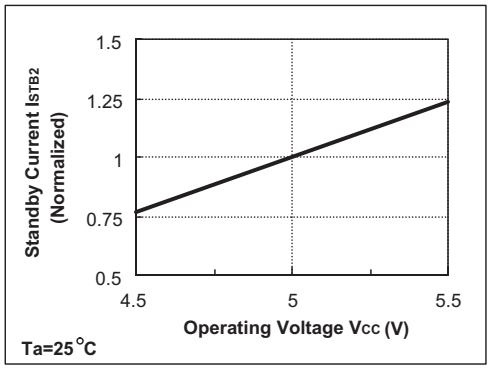

**Propagation Delay Due to Chip and Output Enable (Address Valid)**

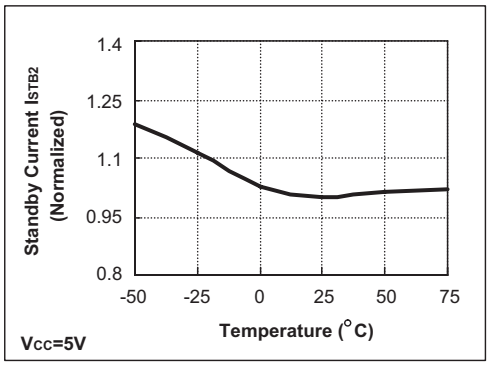


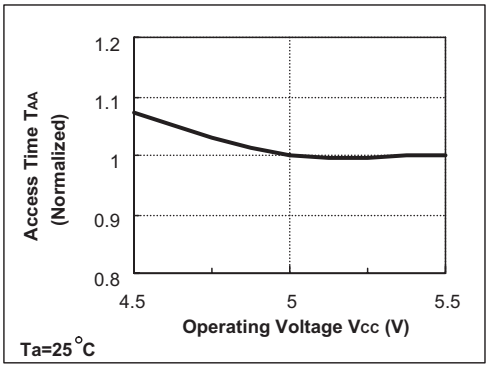

## Characteristic Curves

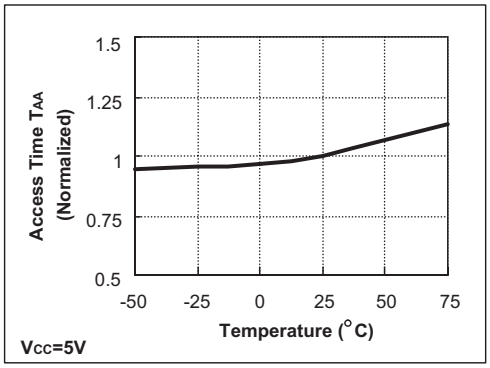


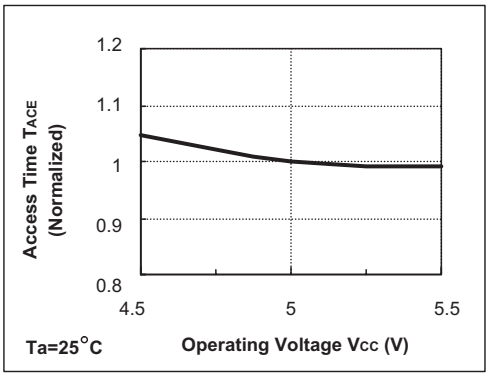



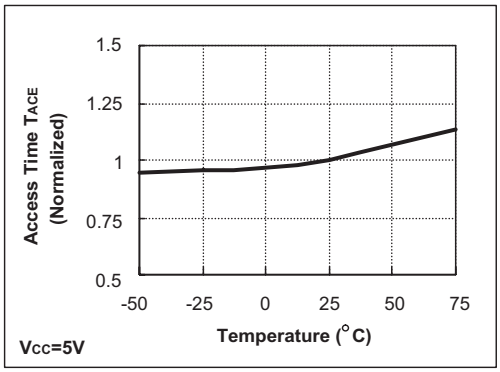



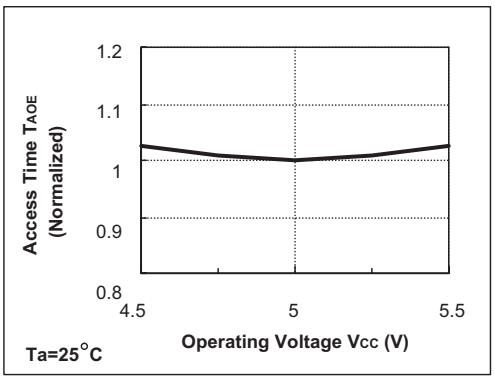



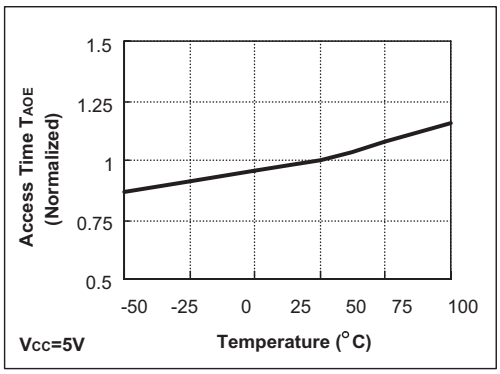

Access Time TAA (Normalized)
1.2
1.1
1
0.9
0.8
4.5
5
5.5
Operating Voltage VCC (V)
Ta=25°C


Access Time TAA (Normalized)
1.5
1.25
1
0.75
0.5
-50
-25
0
25
50
75
Temperature (°C)
VCC=5V


Access Time TACE (Normalized)
1.2
1.1
1
0.9
0.8
4.5
5
5.5
Operating Voltage VCC (V)
Ta=25°C


Access Time TACE (Normalized)
1.5
1.25
1
0.75
0.5
-50
-25
0
25
50
75
Temperature (°C)
VCC=5V


Access Time TAOE (Normalized)
1.2
1.1
1
0.9
0.8
4.5
5
5.5
Operating Voltage VCC (V)
Ta=25°C


Access Time TAOE (Normalized)
1.5
1.25
1
0.75
0.5
-50
-25
0
25
50
75
100
Temperature (°C)
VCC=5V

# HT23C040 Mask ROM Ordering Sheet

**Custom:**_____

**Input Medium:**

☐ EPROM ☐ DISK ☐ File (Mail Address: romfile@holtek.com.tw) ☐ OTHER_____

| User No. | Type/Ref. Name | Q'ty | Check Sum | Memory Address | |
|---|---|---|---|---|---|
| | | | | Start | End |
| | | | | | |

**Control Pin and Package Form Option:**

(a) 32 Pin Type Pin 22:_____ (1) CE (2) $\overline{CE}$ (3) OE1 (4) $\overline{OE1}$

Pin 24:_____ (1) OE (2) $\overline{OE}$ (3) NC

(b) Package Form:_____ (1) Chip Form (2) 32 DIP (3) 32 SOP

**Companion User No.**_____

**Package Marking :**_____

**Delivery Date :**_____ **Q'ty:** _____

**CUSTOM CONFIRMED BY:**

_____

**(NAME, DATE, POSITION & CO. CHOP)**

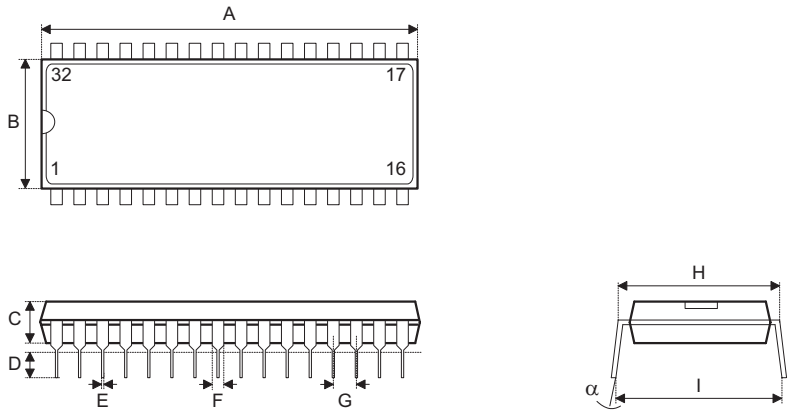
**HOLTEK CONFIRMED BY:**

_____ _____

**(SALES)** **(SALES MANAGER)**

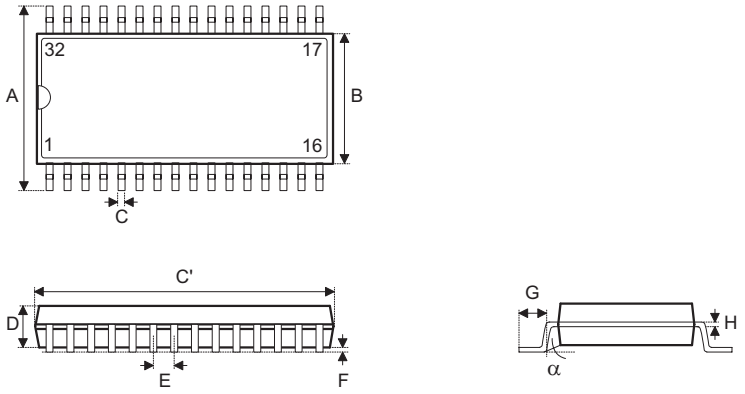
## Package Information

**32-pin DIP (600mil) Outline Dimensions**



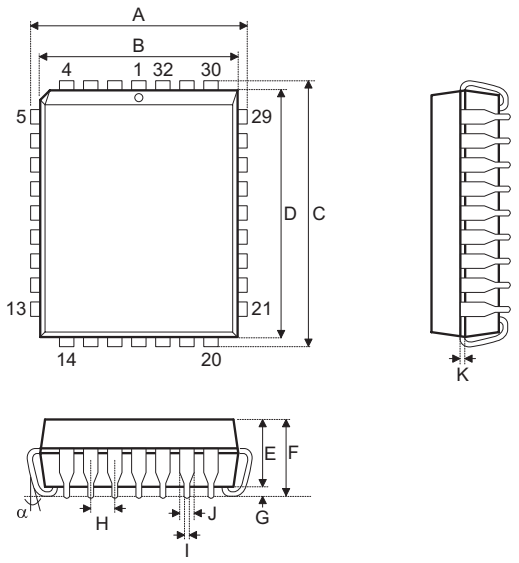

| Symbol | Dimensions in mil | | |
|---|---|---|---|
| | Min. | Nom. | Max. |
| A | 1635 | — | 1665 |
| B | 535 | — | 555 |
| C | 145 | — | 155 |
| D | 125 | — | 145 |
| E | 16 | — | 20 |
| F | 50 | — | 70 |
| G | — | 100 | — |
| H | 595 | — | 615 |
| I | 635 | — | 670 |
| α | 0° | — | 15° |

**32-pin SOP (450mil) Outline Dimensions**




| Symbol | Dimensions in mil | | |
|---|---|---|---|
| | Min. | Nom. | Max. |
| A | 543 | — | 557 |
| B | 440 | — | 450 |
| C | 14 | — | 20 |
| C′ | — | — | 817 |
| D | 100 | — | 112 |
| E | — | 50 | — |
| F | 4 | — | — |
| G | 32 | — | 38 |
| H | 4 | — | 12 |
| α | 0° | — | 10° |

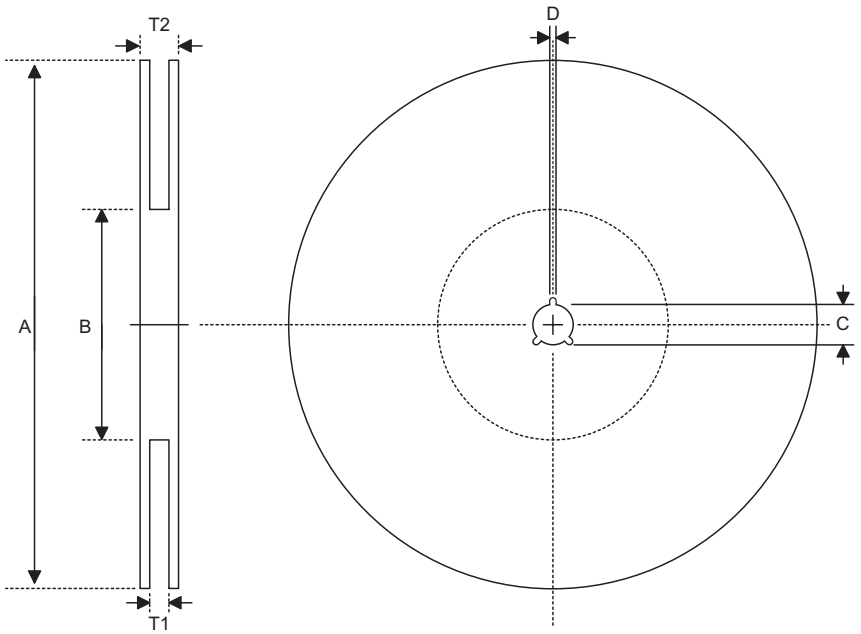
**32-pin PLCC Outline Dimensions**




| Symbol | Dimensions in mil | | |
|---|---|---|---|
| | Min. | Nom. | Max. |
| A | 485 | — | 495 |
| B | 445 | — | 455 |
| C | 585 | — | 595 |
| D | 545 | — | 555 |
| E | 105 | — | 115 |
| F | — | — | 140 |
| G | 15 | — | — |
| H | — | 50 | — |
| I | 16 | — | 22 |
| J | 24 | — | 32 |
| K | 8 | — | 12 |
| α | 0° | — | 10° |

## Product Tape and Reel Specifications

**Reel Dimensions**



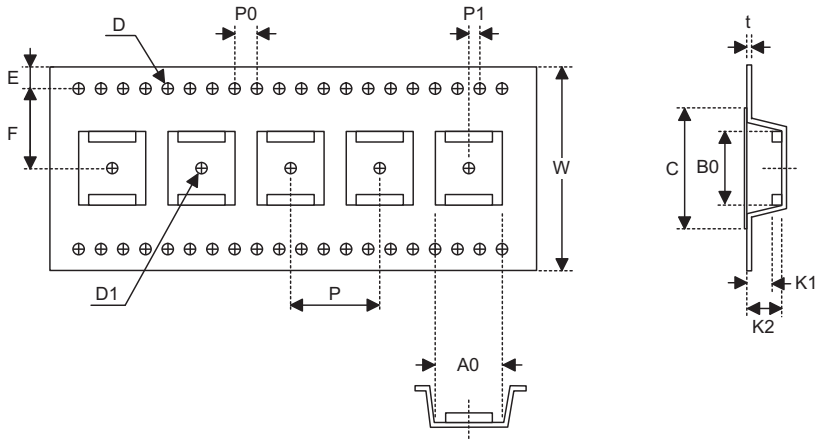

SOP 32W

| Symbol | Description | Dimensions in mm |
|---|---|---|
| A | Reel Outer Diameter | 330±1.0 |
| B | Reel Inner Diameter | 100±0.1 |
| C | Spindle Hole Diameter | 13.0+0.5 −0.2 |
| D | Key Slit Width | 2.0±0.5 |
| T1 | Space Between Flange | 32.8+0.3 −0.2 |
| T2 | Reel Thickness | 38.2+0.2 |

PLCC 32

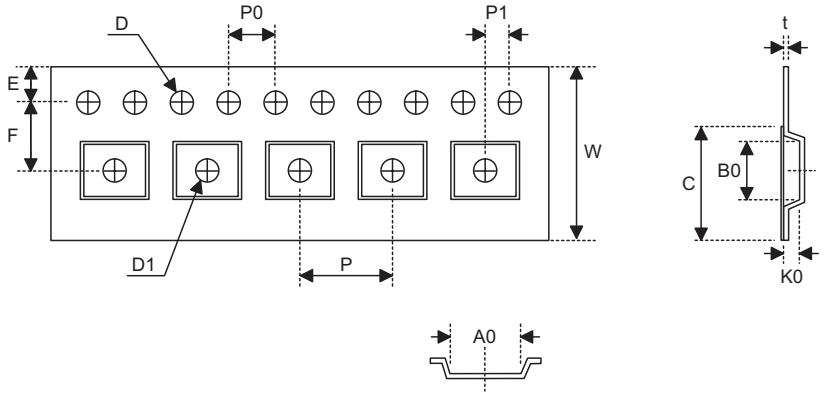
| Symbol | Description | Dimensions in mm |
|---|---|---|
| A | Reel Outer Diameter | 330±1.0 |
| B | Reel Inner Diameter | 62±1.5 |
| C | Spindle Hole Diameter | 13.0+0.5 −0.2 |
| D | Key Slit Width | 2.0±0.5 |
| T1 | Space Between Flange | 24.8+0.3 −0.2 |
| T2 | Reel Thickness | 30.2±0.2 |

**Carrier Tape Dimensions**




SOP 32W

| Symbol | Description | Dimensions in mm |
|---|---|---|
| W | Carrier Tape Width | 32.0+0.3 −0.1 |
| P | Cavity Pitch | 16.0±0.1 |
| E | Perforation Position | 1.75±0.1 |
| F | Cavity to Perforation (Width Direction) | 14.2±0.1 |
| D | Perforation Diameter | 1.55+0.1 |
| D1 | Cavity Hole Diameter | 2.0+0.25 |
| P0 | Perforation Pitch | 4.0±0.1 |
| P1 | Cavity to Perforation (Length Direction) | 2.0±0.1 |
| A0 | Cavity Length | 14.7±0.1 |
| B0 | Cavity Width | 20.9±0.1 |
| K1 | Cavity Depth | 3.0±0.1 |
| K2 | Cavity Depth | 3.4±0.1 |
| t | Carrier Tape Thickness | 0.35±0.05 |
| C | Cover Tape Width | 25.5 |




PLCC 32

| Symbol | Description | Dimensions in mm |
|---|---|---|
| W | Carrier Tape Width | 24.0±0.3 |
| P | Cavity Pitch | 18.0±0.1 |
| E | Perforation Position | 1.75±0.1 |
| F | Cavity to Perforation (Width Direction) | 11.5±0.1 |
| D | Perforation Diameter | 1.5+0.1 |
| D1 | Cavity Hole Diameter | 1.55+1.0 −0.05 |
| P0 | Perforation Pitch | 4.0±0.1 |
| P1 | Cavity to Perforation (Length Direction) | 2.0±0.1 |
| A0 | Cavity Length | 13.1±0.1 |
| B0 | Cavity Width | 15.5±0.1 |
| K0 | Cavity Depth | 3.9±0.1 |
| t | Carrier Tape Thickness | 0.30±0.05 |
| C | Cover Tape Width | 21.3 |

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Fax: 886-2-2655-7373
Fax: 886-2-2655-7383 (International sales hotline)

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http://www.holtek.com.cn

**Holtek Semiconductor Inc. (Shenzhen Sales Office)**
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