

### Features

- Operating voltage: 2.7V~5.5V
- Low power consumption
  - Operation: 25mA max. ( $V_{CC}=5V$ )  
10mA max. ( $V_{CC}=3V$ )
  - Standby: 30 $\mu$ A max. ( $V_{CC}=5V$ )  
10 $\mu$ A max. ( $V_{CC}=3V$ )
- Access time: 150ns max. ( $V_{CC}=5V$ )  
250ns max. ( $V_{CC}=3V$ )
- 65536×8-bit of mask ROM
- Mask options: chip enable  $\overline{CE}/\overline{OE1}/\overline{OE1}$  and output enable  $\overline{OE}/\overline{OE}/\overline{NC}$
- TTL compatible inputs and outputs
- Tristate outputs
- Fully static operation
- 28-pin DIP/SOP package

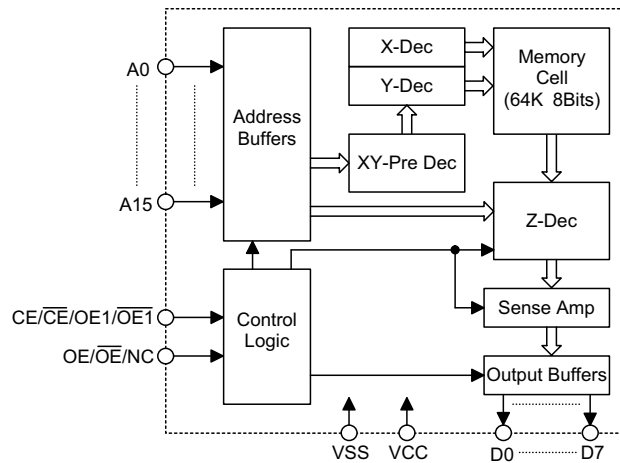
### General Description

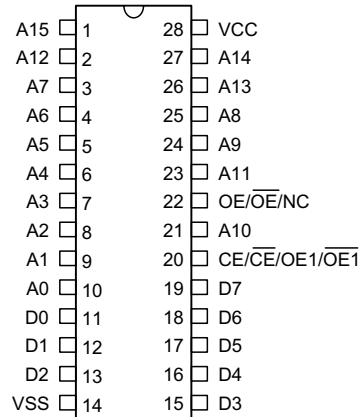
The HT23C512 is a read-only memory with high performance CMOS storage device whose 512K of memory is arranged into 65536 words by 8 bits.

For application flexibility, the chip enable and output enable control pins can be selected as active high or active low. This flexibility not only allows easy interface with most microprocessors, but also eliminates bus conten-

tion in multiple bus microprocessor systems. An additional feature of the HT23C512 is its ability to enter the standby mode whenever the chip enable ( $\overline{CE}/\overline{OE}$ ) is inactive, thus reducing current consumption to below 30 $\mu$ A. The combination of these functions makes the chip suitable for high density low power memory applications.

### Block Diagram



**Pin Assignment**


**HT23C512**  
**- 28 DIP-A/SOP-A**

**Pin Description**

| Pin Name   | I/O | Description                     |
|--|-----|---------------------------------|
| A0~A15   | I   | Address inputs                  |
| D0~D7  | O   | Data outputs                    |
| CE/ $\overline{\text{CE}}$ /OE1/ $\overline{\text{OE1}}$ | I   | Chip enable/Output enable input |
| OE/ $\overline{\text{OE}}$ /NC                           | I   | Output enable input             |
| VSS  | —   | Negative power supply, ground   |
| VCC  | —   | Positive power supply           |

**Absolute Maximum Ratings**

Supply Voltage .....-0.3V to 6V      Storage Temperature .....-50°C to 125°C  
 Input Voltage.....-0.3V to  $V_{CC}+0.3V$       Operating Temperature.....-40°C to 85°C

Note: These are stress ratings only. Stresses exceeding the range specified under "Absolute Maximum Ratings" may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

**D.C. Characteristics**
**Supply voltage: 2.7V~3.6V**

Ta=-40°C to 85°C

| Symbol          | Parameter           | Test Conditions |                         | Min.            | Typ. | Max.            | Unit |
|-----------------|---------------------|-----------------|-------------------------|-----------------|------|-----------------|------|
|                 |                     | V <sub>CC</sub> | Conditions              |                 |      |                 |      |
| V <sub>CC</sub> | Operating Voltage   | —               | —                       | 2.7             | —    | 3.6             | V    |
| I <sub>CC</sub> | Operating Current   | 3V              | O/P Unload, f=5MHz      | —               | —    | 10              | mA   |
| V <sub>IL</sub> | Input Low Voltage   | 3V              | —                       | V <sub>SS</sub> | —    | 0.4             | V    |
| V <sub>IH</sub> | Input High Voltage  | 3V              | —                       | 2.0             | —    | V <sub>CC</sub> | V    |
| V <sub>OL</sub> | Output Low Voltage  | 3V              | I <sub>OL</sub> =2.1mA  | —               | —    | 0.4             | V    |
| V <sub>OH</sub> | Output High Voltage | 3V              | I <sub>OH</sub> =-0.4mA | 2.4             | —    | V <sub>CC</sub> | V    |

| Symbol            | Parameter                     | Test Conditions |   | Min. | Typ. | Max. | Unit |
|-------------------|-------------------------------|-----------------|---|------|------|------|------|
|                   |                               | V <sub>CC</sub> | Conditions  |      |      |      |      |
| I <sub>LI</sub>   | Input Leakage Current         | 3V              | V <sub>IN</sub> =0 to V <sub>CC</sub>                 | —    | —    | 10   | μA   |
| I <sub>LO</sub>   | Output Leakage Current        | 3V              | V <sub>OUT</sub> =0 to V <sub>CC</sub>                | —    | —    | 10   | μA   |
| I <sub>STB1</sub> | Standby Current               | 3V              | CE=V <sub>IL</sub> , $\overline{CE}$ =V <sub>IH</sub> | —    | —    | 500  | μA   |
| I <sub>STB2</sub> | Standby Current               | 3V              | CE ≤ 0.2V, $\overline{CE}$ ≥ V <sub>CC</sub> -0.2V    | —    | —    | 10   | μA   |
| C <sub>IN</sub>   | Input Capacitance (See Note)  | —               | f=1MHz  | —    | —    | 10   | pF   |
| C <sub>OUT</sub>  | Output Capacitance (See Note) | —               | f=1MHz  | —    | —    | 10   | pF   |

Note: These parameters are periodically sampled but not 100% tested.

**Supply voltage: 4.5V~5.5V**

Ta=−40°C to 85°C

| Symbol            | Parameter                     | Test Conditions |   | Min.            | Typ. | Max.            | Unit |
|-------------------|-------------------------------|-----------------|---|-----------------|------|-----------------|------|
|                   |                               | V <sub>CC</sub> | Conditions  |                 |      |                 |      |
| V <sub>CC</sub>   | Operating Voltage             | —               | —   | 4.5             | —    | 5.5             | V    |
| I <sub>CC</sub>   | Operating Current             | 5V              | O/P Unload, f=5MHz                                    | —               | —    | 25              | mA   |
| V <sub>IL</sub>   | Input Low Voltage             | 5V              | —   | V <sub>SS</sub> | —    | 0.8             | V    |
| V <sub>IH</sub>   | Input High Voltage            | 5V              | —   | 2.2             | —    | V <sub>CC</sub> | V    |
| V <sub>OL</sub>   | Output Low Voltage            | 5V              | I <sub>OL</sub> =3.2mA                                | —               | —    | 0.4             | V    |
| V <sub>OH</sub>   | Output High Voltage           | 5V              | I <sub>OH</sub> =−1mA                                 | 2.4             | —    | V <sub>CC</sub> | V    |
| I <sub>LI</sub>   | Input Leakage Current         | 5V              | V <sub>IN</sub> =0 to V <sub>CC</sub>                 | —               | —    | 10              | μA   |
| I <sub>LO</sub>   | Output Leakage Current        | 5V              | V <sub>OUT</sub> =0 to V <sub>CC</sub>                | —               | —    | 10              | μA   |
| I <sub>STB1</sub> | Standby Current               | 5V              | CE=V <sub>IL</sub> , $\overline{CE}$ =V <sub>IH</sub> | —               | —    | 1.5             | mA   |
| I <sub>STB2</sub> | Standby Current               | 5V              | CE ≤ 0.2V, $\overline{CE}$ ≥ V <sub>CC</sub> -0.2V    | —               | —    | 30              | μA   |
| C <sub>IN</sub>   | Input Capacitance (See Note)  | —               | f=1MHz  | —               | —    | 10              | pF   |
| C <sub>OUT</sub>  | Output Capacitance (See Note) | —               | f=1MHz  | —               | —    | 10              | pF   |

Note: These parameters are periodically sampled but not 100% tested.

**A.C. Characteristics**

Ta=−40°C to 85°C

| Symbol           | Parameter                      | V <sub>CC</sub> =2.7V~3.6V |      | V <sub>CC</sub> =4.5V~5.5V |      | Unit |
|------------------|--------------------------------|----------------------------|------|----------------------------|------|------|
|                  |                                | Min.                       | Max. | Min.                       | Max. |      |
| t <sub>CYC</sub> | Cycle Time                     | 250                        | —    | 150                        | —    | ns   |
| t <sub>AA</sub>  | Address Access Time            | —                          | 250  | —                          | 150  | ns   |
| t <sub>ACE</sub> | Chip Enable Access Time        | —                          | 250  | —                          | 150  | ns   |
| t <sub>AOE</sub> | Output Enable Access Time      | —                          | 150  | —                          | 80   | ns   |
| t <sub>OH</sub>  | Output Hold Time               | —                          | —    | 10                         | —    | ns   |
| t <sub>OD</sub>  | Output Disable Time (See Note) | —                          | —    | —                          | 70   | ns   |
| t <sub>OE</sub>  | Output Enable Time (See Note)  | —                          | —    | 10                         | —    | ns   |

Note: These parameters are periodically sampled but not 100% tested.

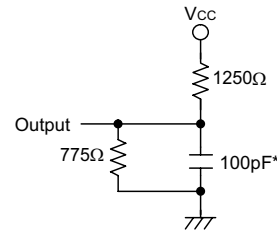
**A.C. test conditions**

Output load: see figure right

Input rise and fall time: 10ns

Input pulse levels: 0.4V to 2.4V

Input and output timing reference levels:  
0.8V and 2.0V ( $V_{CC}=5V$ ), 1.5V ( $V_{CC}=3V$ )



\* Including scope and jig  
Output load circuit

**Functional Description**

The HT23C512 has two modes, namely data read mode and standby mode, controlled by  $\overline{CE}/\overline{CE}/\overline{OE1}/\overline{OE1}$  and  $\overline{OE}/\overline{OE}/\overline{NC}$  inputs.

• Standby mode

The HT23C512 has lower current consumption, controlled by the chip enable input ( $\overline{CE}/\overline{CE}$ ). When a low/high level is applied to the  $\overline{CE}/\overline{CE}$  input regardless of the output enable ( $\overline{OE}/\overline{OE}/\overline{NC}$ ) states, the chip will enter the standby mode.

• Data read mode

When both the chip enable ( $\overline{CE}/\overline{CE}/\overline{OE1}/\overline{OE1}$ ) and the output enable ( $\overline{OE}/\overline{OE}/\overline{NC}$ ) are active, the chip is in data read mode. Otherwise, active  $\overline{CE}/\overline{CE}$  and inactive  $\overline{OE}/\overline{OE}/\overline{NC}$  result in deselect mode. The output will remain in Hi-Z state.

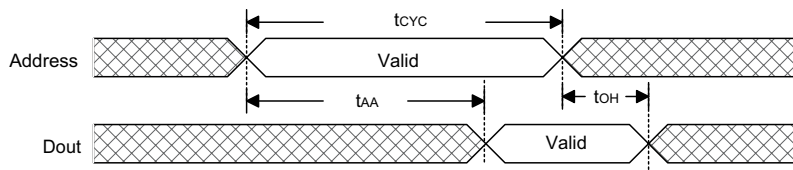
**Operation Truth Table**

| Mode     | $\overline{CE}/\overline{CE}$ | $\overline{OE}/\overline{OE}$ | A0~A15 | D0~D7    |
|----------|-------------------------------|-------------------------------|--------|----------|
| Read     | H/L                           | H/L                           | Valid  | Data Out |
| Deselect | H/L                           | L/H                           | X      | High Z   |
| Standby  | L/H                           | X                             | X      | High Z   |

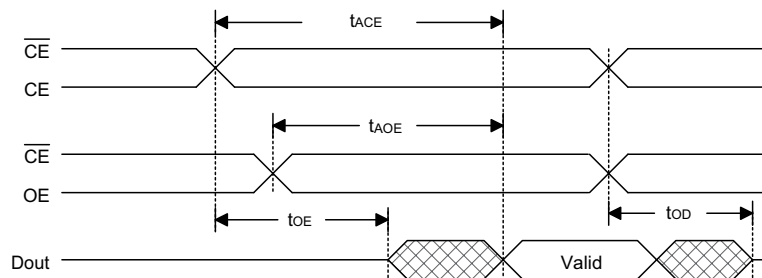
Note: H= $V_{IH}$ , L= $V_{IL}$ , X= $V_{IH}$  or  $V_{IL}$

**Timing Diagrams**

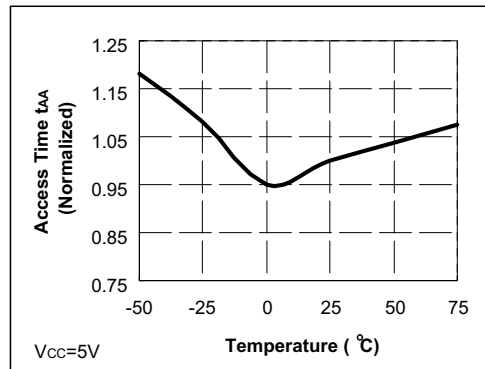
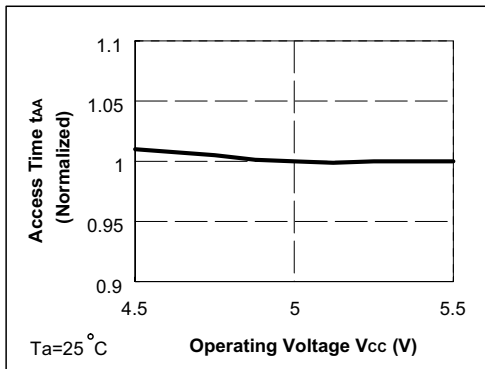
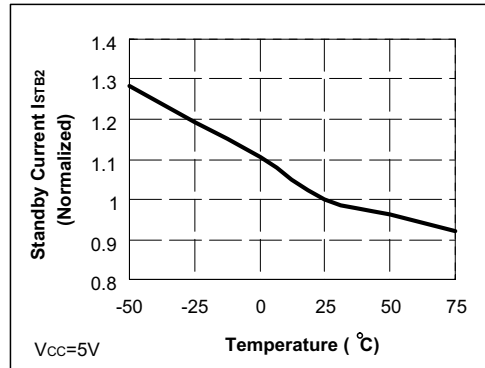
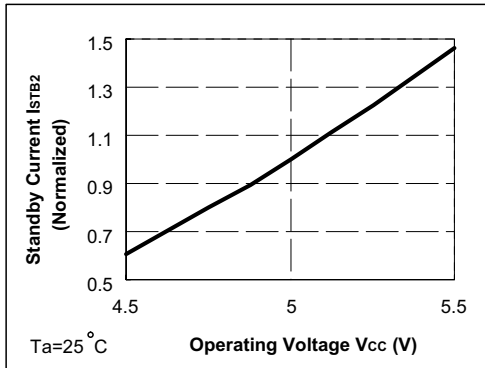
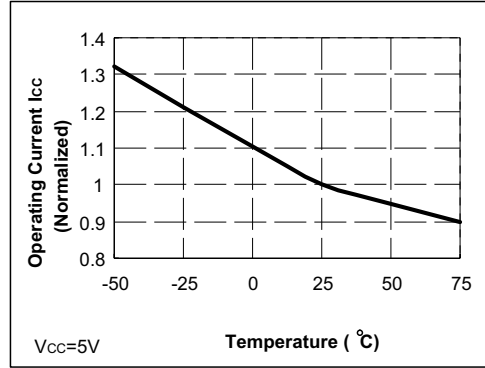
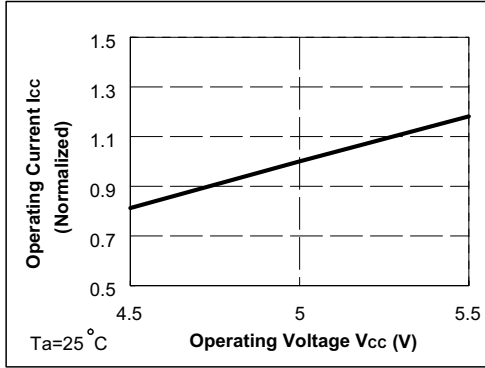
- Propagation delay due to address ( $\overline{CE}/\overline{CE}/\overline{OE1}/\overline{OE1}$  and  $\overline{OE}/\overline{OE}$  are active)

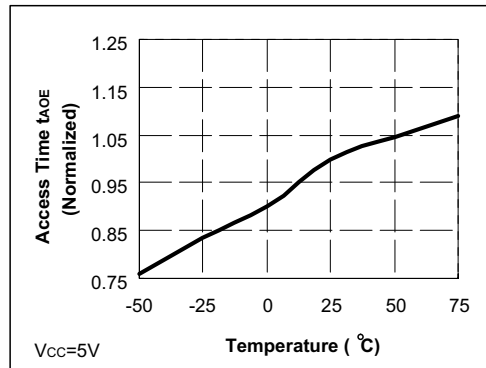
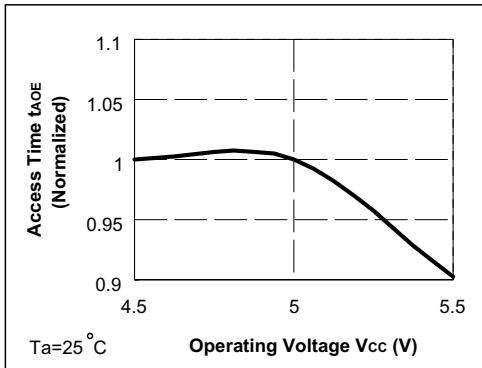
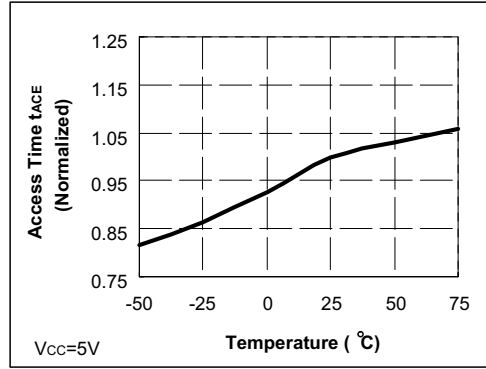
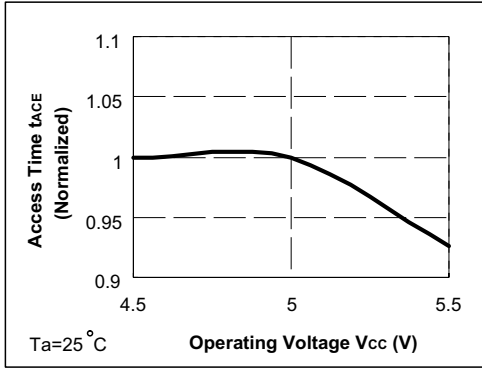


- Propagation delay due to chip enable and output enable (address valid)



Characteristic Curves





## HT23C512 MASK ROM ORDERING SHEET

Custom: \_\_\_\_\_

**Input Medium:**

EPROM  
  DISK  
  File (Mail Address: romfile@holtek.com.tw)  
  OTHER \_\_\_\_\_

| User No. | Type/Ref. Name | Q'ty | Check Sum | Memory Address |     |
|----------|----------------|------|-----------|----------------|-----|
|          |                |      |           | Start          | End |
|          |                |      |           |                |     |

**Control Pin and Package Form Option:**

(a) 28 Pin Type Pin 20: \_\_\_\_\_ (1) CE (2) CE (3) OE1 (4) OE1

Pin 22: \_\_\_\_\_ (1) OE (2) OE (3) NC

(b) Package Form: \_\_\_\_\_ (1) Chip Form (2) 28 DIP (3) 28 SOP

Companion User No. \_\_\_\_\_

Package Marking : \_\_\_\_\_

Delivery Date : \_\_\_\_\_ Q'ty: \_\_\_\_\_

**CUSTOM CONFIRMED BY:**

\_\_\_\_\_  
(NAME, DATE, POSITION & CO. CHOP)

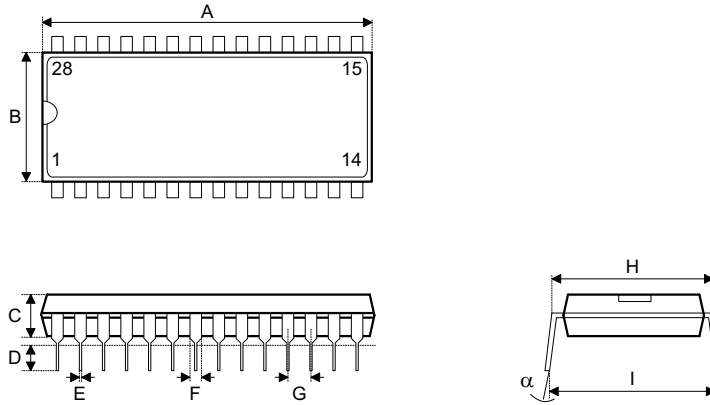
**HOLTEK CONFIRMED BY:**

\_\_\_\_\_  
(SALES)

\_\_\_\_\_  
(SALES MANAGER)

**Package Information**

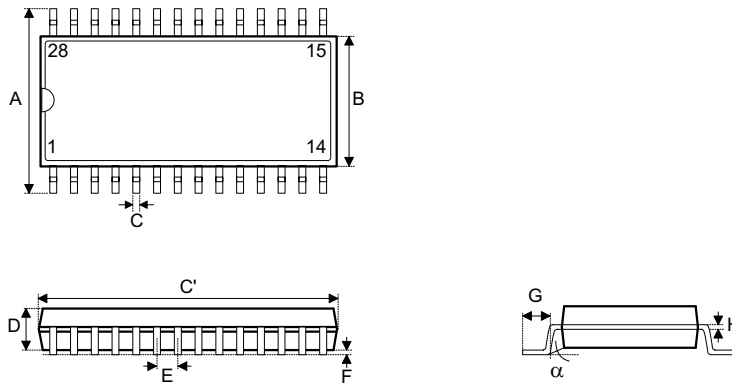
28-pin DIP (600mil) outline dimensions



| Symbol   | Dimensions in mil |      |      |
|----------|-------------------|------|------|
|          | Min.              | Nom. | Max. |
| A        | 1445              | —    | 1465 |
| B        | 535               | —    | 555  |
| C        | 145               | —    | 155  |
| D        | 125               | —    | 145  |
| E        | 16                | —    | 20   |
| F        | 50                | —    | 70   |
| G        | —                 | 100  | —    |
| H        | 595               | —    | 615  |
| I        | 635               | —    | 670  |
| $\alpha$ | 0°                | —    | 15°  |



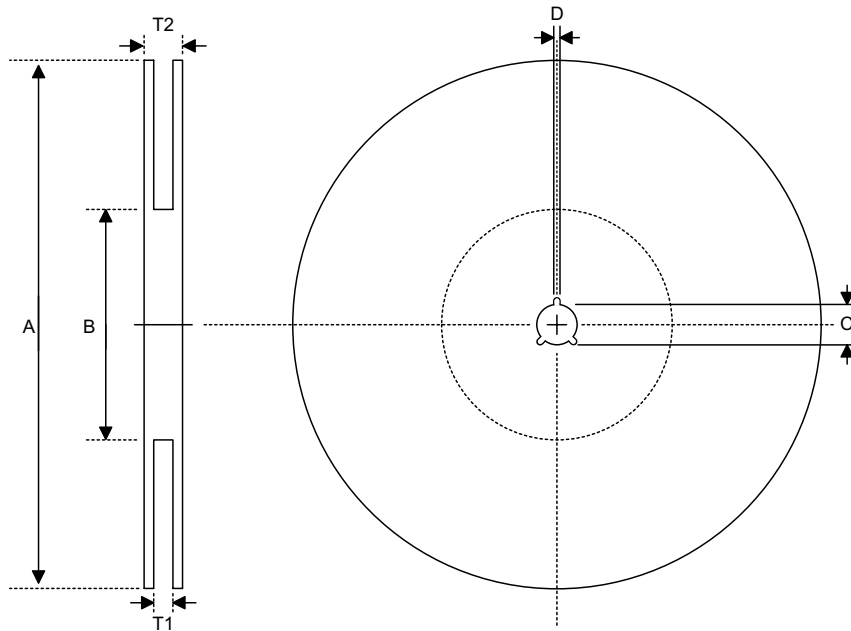
**28-pin SOP (300mil) outline dimensions**



| Symbol   | Dimensions in mil |      |      |
|----------|-------------------|------|------|
|          | Min.              | Nom. | Max. |
| A        | 394               | —    | 419  |
| B        | 290               | —    | 300  |
| C        | 14                | —    | 20   |
| C'       | 697               | —    | 713  |
| D        | 92                | —    | 104  |
| E        | —                 | 50   | —    |
| F        | 4                 | —    | —    |
| G        | 32                | —    | 38   |
| H        | 4                 | —    | 12   |
| $\alpha$ | 0°                | —    | 10°  |

**Product Tape and Reel Specifications**

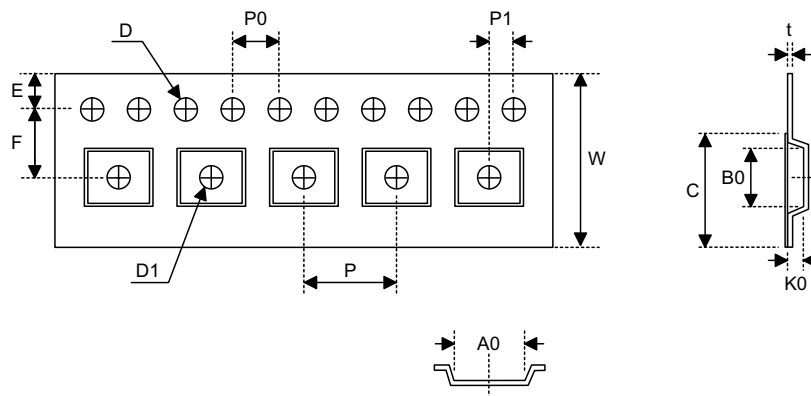
**Reel dimensions**



SOP 28W (300mil)

| Symbol | Description           | Dimensions in mm |
|--------|-----------------------|------------------|
| A      | Reel Outer Diameter   | 330±1.0          |
| B      | Reel Inner Diameter   | 62±1.5           |
| C      | Spindle Hole Diameter | 13.0+0.5<br>-0.2 |
| D      | Key Slit Width        | 2.0±0.5          |
| T1     | Space Between Flange  | 24.8+0.3<br>-0.2 |
| T2     | Reel Thickness        | 30.2±0.2         |

**Carrier tape dimensions**



SOP 28W (300mil)

| Symbol | Description                              | Dimensions in mm |
|--------|--|------------------|
| W      | Carrier Tape Width                       | 24.0±0.3         |
| P      | Cavity Pitch                             | 12.0±0.1         |
| E      | Perforation Position                     | 1.75±0.1         |
| F      | Cavity to Perforation (Width Direction)  | 11.5±0.1         |
| D      | Perforation Diameter                     | 1.5+0.1          |
| D1     | Cavity Hole Diameter                     | 1.5+0.25         |
| P0     | Perforation Pitch                        | 4.0±0.1          |
| P1     | Cavity to Perforation (Length Direction) | 2.0±0.1          |
| A0     | Cavity Length                            | 10.85±0.1        |
| B0     | Cavity Width                             | 18.34±0.1        |
| K0     | Cavity Depth                             | 2.97±0.1         |
| t      | Carrier Tape Thickness                   | 0.35±0.01        |
| C      | Cover Tape Width                         | 21.3             |

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