HT27LC010
CMOS 128K×8-Bit OTP EPROM

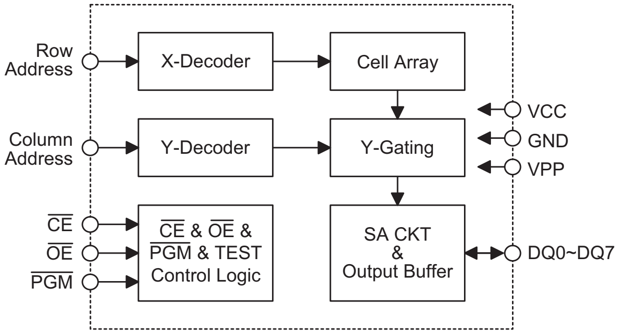
Features

- Operating voltage: +3.3V
- Programming voltage
  - V_{PP}=12.5V±0.2V
  - V_{CC}=6.0V±0.2V
- High-reliability CMOS technology
- Latch-up immunity to 100mA from -1.0V to V_{CC}+1.0V
- CMOS and TTL compatible I/O
- Low power consumption
  - Active: 15mA max.
  - Standby: 1μA typ.
- 128K×8-bit organization
- Fast read access time: 90ns
- Fast programming algorithm
- Programming time 75μs typ.
- Two line controls ($\overline{OE}$ and $\overline{CE}$)
- Standard product identification code
- Commercial temperature ranges (0°C to +70°C)
- 32-pin DIP/SOP/TSOP/PLCC Package

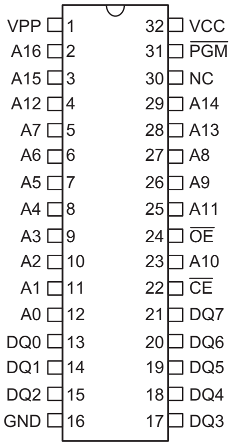
General Description

The HT27LC010 chip family is a low-power, 1024K (1,048,576) bit, +3.3V electrically one-time programmable (OTP) read-only memories (EPROM). Organized into 128K words with 8 bits per word, it features a fast single address location programming, typically at 75μs per byte. Any byte can be accessed in less than 90ns with respect to Spec. This eliminates the need for WAIT states in high-performance microprocessor systems. The HT27LC010 has separate Output Enable ($\overline{OE}$) and Chip Enable ($\overline{CE}$) controls which eliminate bus contention issues.

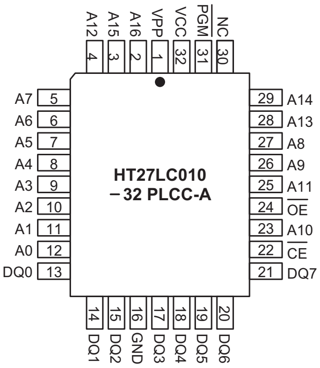
Block Diagram



Pin Assignment



HT27LC010
– 32 DIP-A/SOP-A



Pin Description

Pin Name	I/O/C/P	Description
VPP	P	Program voltage supply
A0~A16	I	Address inputs
DQ0~DQ7	I/O	Data inputs/outputs
$\overline{\text{CE}}$	C	Chip enable
$\overline{\text{OE}}$	C	Output enable
$\overline{\text{PGM}}$	C	Program strobe
NC	—	No connection
VCC	—	Positive power supply

Absolute Maximum Rating

Operation Temperature Commercial ....0°C to +70°C

Storage Temperature ....–65°C to 125 °C

Applied VCC Voltage with Respect to GND .... –0.6V to 7.0V

Applied Voltage on Input Pin with Respect to GND .... –0.6V to 7.0V

Applied Voltage on Output Pin with Respect to GND .... –0.6V to V_{CC}+0.5V

Applied Voltage on A9 Pin with Respect to GND .... –0.6V to 13.5V

Applied VPP Voltage with Respect to GND ....–0.6V to 13.5V

Applied READ Voltage (Functionality is guaranteed between these limits) ....+3.0V to +3.6V

Note: These are stress ratings only. Stresses exceeding the range specified under "Absolute Maximum Ratings" may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

D.C. Characteristics

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{CC}	Conditions				
Read Operation							
V_{OH}	Output High Level	3.3V	I_{OH}=–0.4mA	2.4	—	—	V
V_{OL}	Output Low Level	3.3V	I_{OL}=2.0mA	—	—	0.45	V
V_{IH}	Input High Level	3.3V	—	2.0	—	V_{CC}+0.5	V
V_{IL}	Input Low Level	3.3V	—	–0.3	—	0.8	V
I_{LI}	Input Leakage Current	3.3V	V_{IN}=0 to 3.6V	–5	—	5	μA
I_{LO}	Output Leakage Current	3.3V	V_{OUT}=0 to 3.6V	–10	—	10	μA
I_{CC}	VCC Active Current	3.3V	$\overline{CE}$=V_{IL}, f=5MHz, I_{OUT}=0mA	—	—	15	mA
I_{SB1}	Standby Current (CMOS)	3.3V	$\overline{CE}$=V_{CC}±0.3V	—	1.0	10	μA
I_{SB2}	Standby Current (TTL)	3.3V	$\overline{CE}$=V_{IH}	—	—	0.6	mA
I_{PP}	VPP Read/Standby Current	3.3V	$\overline{CE}$=$\overline{OE}$=V_{IL}, V_{PP}=V_{CC}	—	—	100	μA
Programming Operation							
V_{OH}	Output High Level	6V	I_{OH}=–0.4mA	2.4	—	—	V
V_{OL}	Output Low Level	6V	I_{OL}=2.0mA	—	—	0.45	V
V_{IH}	Input High Level	6V	—	0.7V_{CC}	—	V_{CC}+0.5	V
V_{IL}	Input Low Level	6V	—	–0.5	—	0.8	V
I_{LI}	Input Load Current	6V	V_{IN}=V_{IL}, V_{IH}	—	—	5.0	μA
V_H	A9 Product ID Voltage	6V	—	11.5	—	12.5	V
I_{CC}	VCC Supply Current	6V	—	—	—	40	mA
I_{PP}	VPP Supply Current	6V	$\overline{CE}$=V_{IL}	—	—	10	mA
Capacitance							
C_{IN}	Input Capacitance	3.3V	V_{IN}=0V	—	8	12	pF
C_{OUT}	Output Capacitance	3.3V	V_{OUT}=0V	—	8	12	pF
C_{VPP}	VPP Capacitance	3.3V	V_{PP}=0V	—	18	25	pF

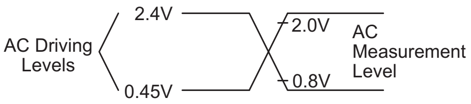
A.C. Characteristics

Ta=+25°C±5°C

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{CC}	Conditions				
Read Operation							
t_{ACC}	Address to Output Delay	3.3V	$\overline{CE}$=$\overline{OE}$=V_{IL}	—	—	90	ns
t_{CE}	Chip Enable to Output Delay	3.3V	$\overline{OE}$=V_{IL}	—	—	90	ns
t_{OE}	Output Enable to Output Delay	3.3V	$\overline{CE}$=V_{IL}	—	—	45	ns
t_{DF}	$\overline{CE}$ or $\overline{OE}$ High to Output Float, Whichever Occurred First	3.3V	—	—	—	40	ns
t_{OH}	Output Hold from Address, $\overline{CE}$ or $\overline{OE}$, Whichever Occurred First	3.3V	—	0	—	—	ns

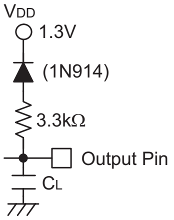
Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{CC}	Conditions				
Programming Operation							
t_{AS}	Address Setup Time	6V	—	2	—	—	μs
t_{OES}	$\overline{OE}$ Setup Time	6V	—	2	—	—	μs
t_{DS}	Data Setup Time	6V	—	2	—	—	μs
t_{AH}	Address Hold Time	6V	—	0	—	—	μs
t_{DH}	Data Hold Time	6V	—	2	—	—	μs
t_{DFP}	Output Enable to Output Float Delay	6V	—	0	—	130	ns
t_{VPS}	VPP Setup Time	6V	—	2	—	—	μs
t_{PW}	$\overline{PGM}$ Program Pulse Width	6V	—	30	75	105	μs
t_{VCS}	VCC Setup Time	6V	—	2	—	—	μs
t_{CES}	$\overline{CE}$ Setup Time	6V	—	2	—	—	μs
t_{OE}	Data Valid from $\overline{OE}$	6V	—	—	—	150	ns
t_{PRT}	VPP Pulse Rise Time During Programming	6V	—	2	—	—	μs

Test Waveforms and Measurements



t_R, t_F< 20ns (10% to 90%)

Output Test Load



Note: C_L=100pF including jig capacitance.

Product Identification Code

Code	Pins										Hex Data
	A0	A1	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	
Manufacturer	0	1	0	0	0	1	1	1	0	0	1C
Device Type	1	1	0	0	0	0	0	0	0	1	01
Continuation	0	0	0	1	1	1	1	1	1	1	7F
	1	0	0	1	1	1	1	1	1	1	7F

Functional Description

Operation Mode

All the operation modes are shown in the table following.

Mode	$\overline{\text{CE}}$	$\overline{\text{OE}}$	$\overline{\text{PGM}}$	A0	A1	A9	VPP	Output
Read	V_{IL}	V_{IL}	X (2)	X	X	X	V_{CC}	Dout
Output Disable	V_{IL}	V_{IH}	X	X	X	X	V_{CC}	High Z
Standby (TTL)	V_{IH}	X	X	X	X	X	V_{CC}	High Z
Standby (CMOS)	$V_{CC}\pm 0.3V$	X	X	X	X	X	V_{CC}	High Z
Program	V_{IL}	V_{IH}	V_{IL}	X	X	X	V_{PP}	D_{IN}
Program Verify	V_{IL}	V_{IL}	V_{IH}	X	X	X	V_{PP}	D_{OUT}
Product Inhibit	V_{IH}	X	X	X	X	X	V_{PP}	High Z
Manufacturer Code (3)	V_{IL}	V_{IL}	X	V_{IL}	V_{IH}	V_H (1)	V_{CC}	1C
Device Code (3)	V_{IL}	V_{IL}	X	V_{IH}	V_{IH}	V_H (1)	V_{CC}	01

Notes: (1) ″V_H″ 12.0V ± 0.5V

(2) ″X″ Either V_{IH} or V_{IL}

(3) For Manufacturer Code and Device Code, A1=V_{IH}, When A1=V_{IL}, both codes will read 7F

Programming of the HT27LC010

When the HT27LC010 is delivered, the chip has all 1024K bits in the ″ONE″, or HIGH state. ″ZEROs″ are loaded into the HT27LC010 through programming.

The programming mode is entered when 12.5±0.2V is applied to the VPP pin, $\overline{\text{OE}}$ is at V_{IH}, and $\overline{\text{CE}}$ and $\overline{\text{PGM}}$ are V_{IL}. For programming, the data to be programmed is applied with 8 bits in parallel to the data pins.

The programming flowchart in Figure 3 shows the fast interactive programming algorithm. The interactive algorithm reduces programming time by using 30μs to 105μs programming pulses and giving each address only as many pulses as is necessary in order to reliably program the data. After each pulse is applied to a given address, the data in that address is verified. If the data is not verified, additional pulses are given until it is verified or until the maximum number of pulses is reached while sequencing through each address of the HT27LC010. This process is repeated while sequencing through each address of the HT27LC010. This part of the programming algorithm is done at V_{CC}=6.0V to assure that each EPROM bit is programmed to a sufficiently high threshold voltage. This ensures that all bits have sufficient margin. After the final address is completed, the entire EPROM memory is read at V_{CC}=V_{PP}=3.3±0.3V to verify the entire memory.

Program Inhibit Mode

Programming of multiple HT27LC010 in parallel with different data is also easily accomplished by using the Program Inhibit Mode. Except for $\overline{\text{CE}}$, all like inputs of the parallel HT27LC010 may be common. A TTL low-level program pulse applied to an HT27LC010 $\overline{\text{CE}}$ input with Vpp=12.5±0.2V, $\overline{\text{PGM}}$ LOW, and $\overline{\text{OE}}$ HIGH will program that HT27LC010. A high-level CE input inhibits the HT27LC010 from being programmed.

Program Verify Mode

Verification should be performed on the programmed bits to determine whether they were correctly programmed. The verification should be performed with $\overline{\text{OE}}$ and $\overline{\text{CE}}$ at V_{IL}, $\overline{\text{PGM}}$ at V_{IH}, and VPP at its programming voltage.

Auto Product Identification

The Auto Product Identification mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and the type. This mode is intended for programming to automatically match the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C±5°C ambient temperature range that is required when programming the HT27LC010.

To activate this mode, the programming equipment must force 12.0±0.5V on the address line A9 of the HT27LC010. Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 from V_{IL} to V_{IH}, when A1=V_{IH}. All other address lines must be held at V_{IH} during Auto Product Identification mode.

Byte 0 (A0=V_{IL}) represents the manufacturer code, and byte 1 (A0=V_{IH}), the device code. For HT27LC010, these two identifier bytes are given in the Mode Select Table. All identifiers for the manufacturer and device codes will possess odd parity, with the MSB (DQ7) defined as the parity bit. When A1=V_{IL}, the HT27LC010 will read out the binary code of 7F, continuation code, to signify the unavailability of manufacturer ID codes.

Read Mode

The HT27LC010 has two control functions, both of which must be logically satisfied in order to obtain data at outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs (t_{OE}) after the falling edge of $\overline{OE}$, assuming the $\overline{CE}$ has been LOW and addresses have been stable for at least t_{ACC}-t_{OE}.

Standby Mode

The HT27LC010 has CMOS standby mode which reduces the maximum VCC current to 10μA. It is placed in CMOS standby when $\overline{CE}$ is at V_{CC}±0.3V. The HT27LC010 also has a TTL-standby mode which reduces the maximum VCC current to 0.6mA. It is placed in TTL-standby when $\overline{CE}$ is at V_{IH}. When in standby mode, the outputs are in a high-impedance state, independent of the $\overline{OE}$ input.

Two-line Output Control Function

To accommodate multiple memory connections, a two-line control function is provided to allow for:

- Low memory power dissipation
- Assurance that output bus contention will not occur

It is recommended that $\overline{CE}$ be decoded and used as the primary device-selection function, while $\overline{OE}$ be made a common connection to the READ line from the system control bus. This assures that all deselected memory devices are in their low-power standby mode and that the output pins are only active when data is desired from a particular memory device.

System Considerations

During the switch between active and standby conditions, transient current peaks are produced on the rising and falling edges of Chip Enable. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. At a minimum, a 0.1μF ceramic capacitor (high frequency, low inherent inductance) should be used on each device between VCC and VPP to minimize transient effects. In addition, to overcome the voltage drop caused by the inductive effects of the printed circuit board traces on EPROM arrays, a 4.7μF bulk electrolytic capacitor should be used between VCC and VPP for each eight devices. The location of the capacitor should be close to where the power supply is connected to the array.

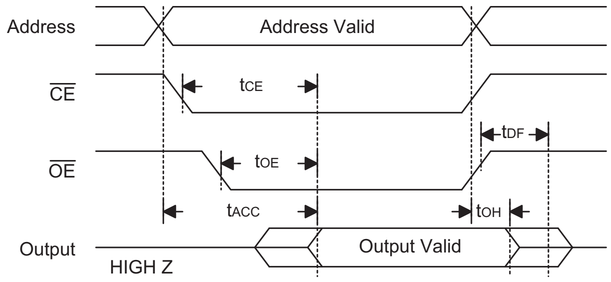


Figure 1. A.C. Waveforms for Read Operation

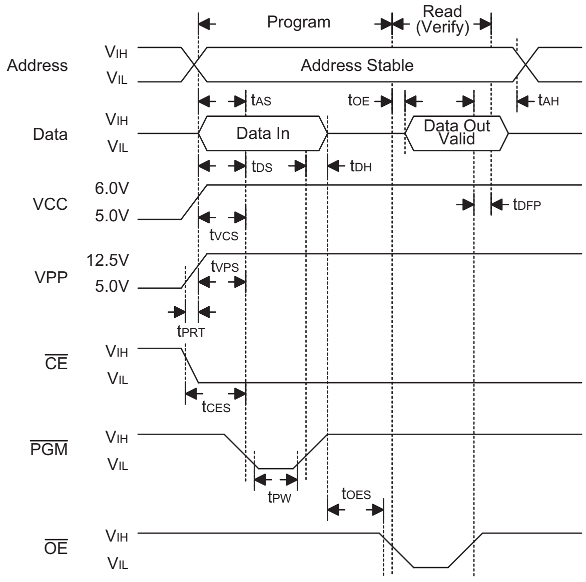
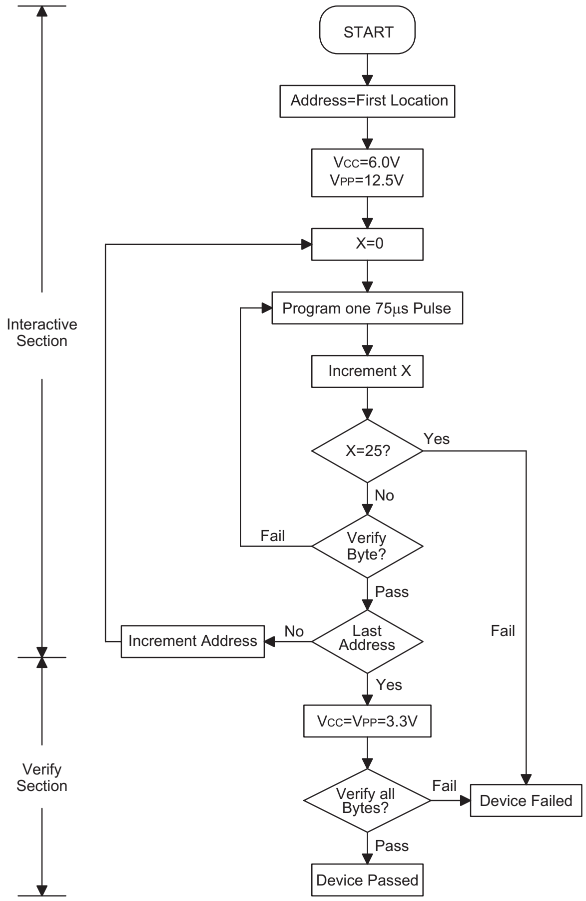


Figure 2. Programming Waveforms

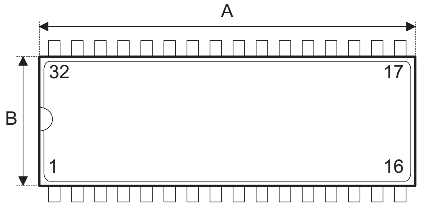


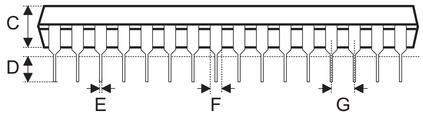
Note: Either 105µs or 30µs pulse.

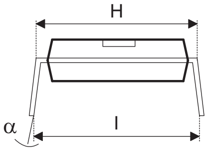
Figure 3. Fast Programming Flowchart

Package Information

32-pin DIP (600mil) Outline Dimensions

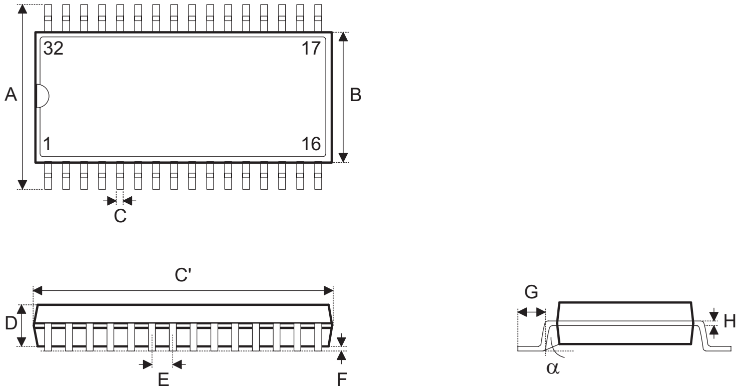






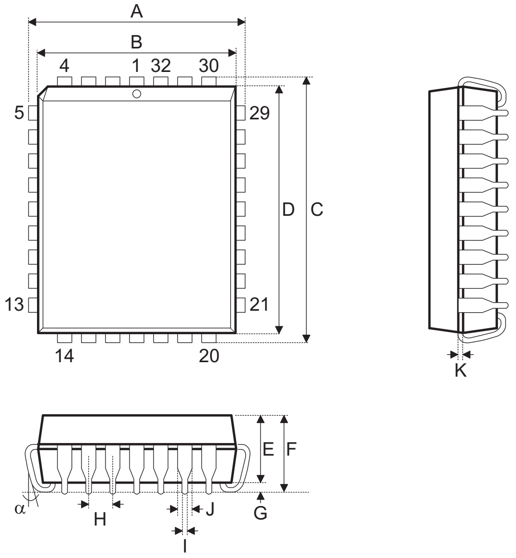
Symbol	Dimensions in mil		
	Min.	Nom.	Max.
A	1635	—	1665
B	535	—	555
C	145	—	155
D	125	—	145
E	16	—	20
F	50	—	70
G	—	100	—
H	595	—	615
I	635	—	670
α	0°	—	15°

32-pin SOP (450mil) Outline Dimensions



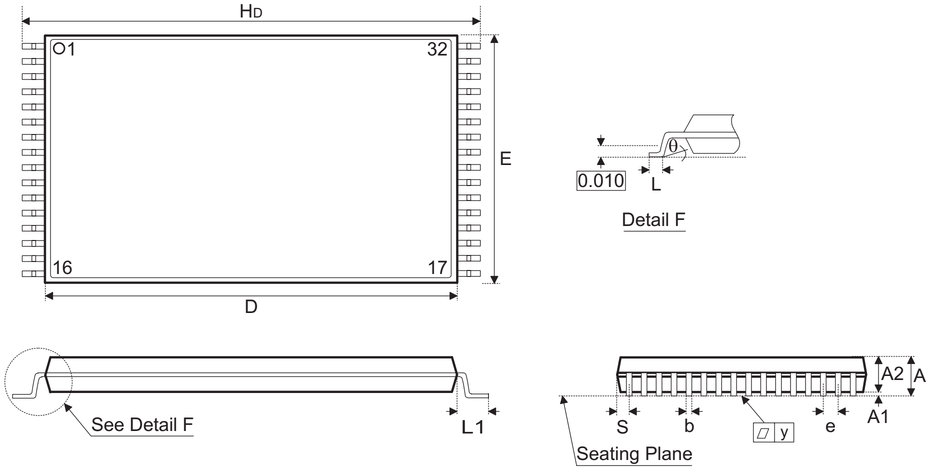
Symbol	Dimensions in mil		
	Min.	Nom.	Max.
A	543	—	557
B	440	—	450
C	14	—	20
C′	—	—	817
D	100	—	112
E	—	50	—
F	4	—	—
G	32	—	38
H	4	—	12
α	0°	—	10°

32-pin PLCC Outline Dimensions



Symbol	Dimensions in mil		
	Min.	Nom.	Max.
A	485	—	495
B	445	—	455
C	585	—	595
D	545	—	555
E	105	—	115
F	—	—	140
G	15	—	—
H	—	50	—
I	16	—	22
J	24	—	32
K	8	—	12
α	0°	—	10°

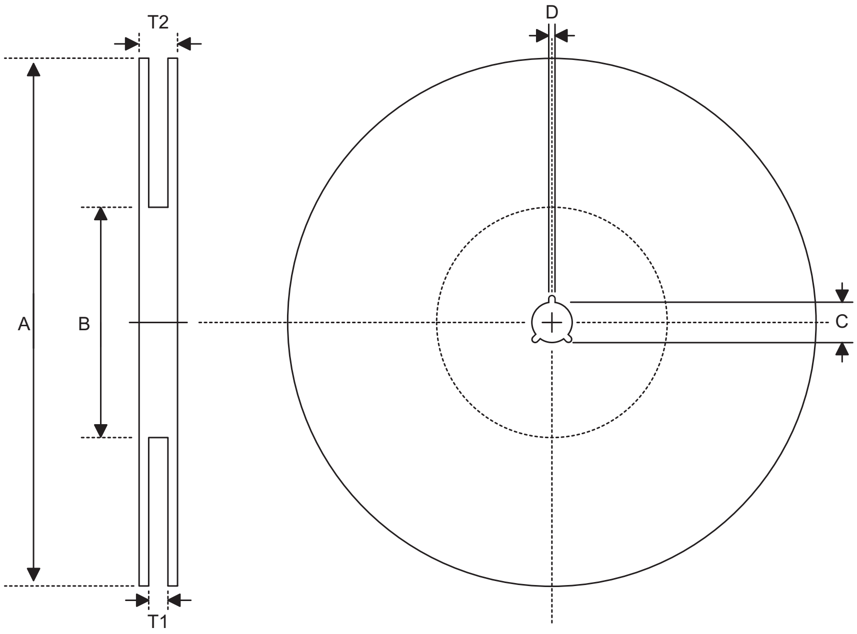
32-pin TSOP (8×20) Outline Dimensions



Symbol	Dimensions in mm		
	Min.	**Nom.**	**Max.**
A	—	—	1.20
A1	0.05	—	0.15
A2	0.95	—	1.05
b	—	0.22	—
D	18.30	—	18.50
H_D	19.80	—	20.20
E	7.90	—	8.10
e	—	0.50	—
L	—	0.60	—
L1	—	0.80	—
θ	0°	—	5°

Product Tape and Reel Specifications

Reel Dimensions



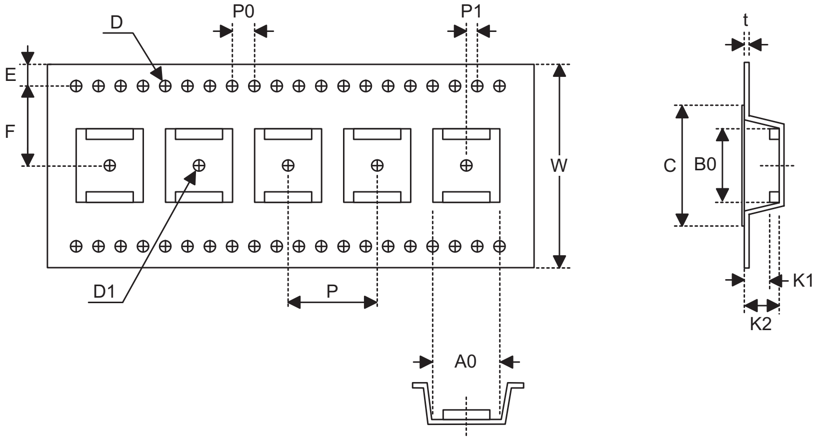
SOP 32W

Symbol	Description	Dimensions in mm
A	Reel Outer Diameter	330±1.0
B	Reel Inner Diameter	100±0.1
C	Spindle Hole Diameter	13.0+0.5 −0.2
D	Key Slit Width	2.0±0.5
T1	Space Between Flange	32.8+0.3 −0.2
T2	Reel Thickness	38.2+0.2

PLCC 32

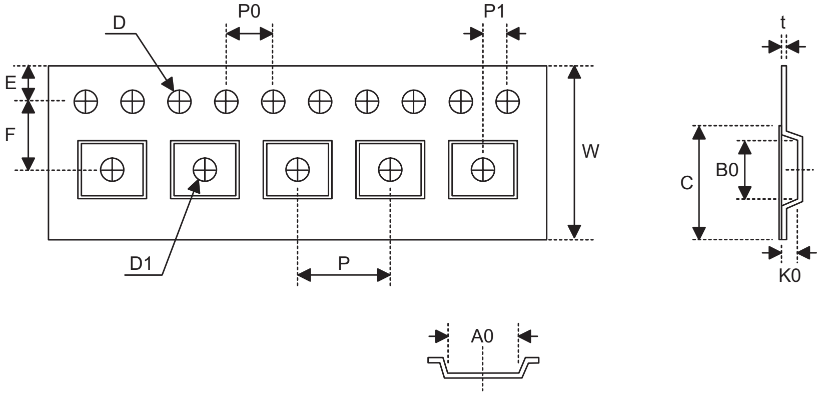
Symbol	Description	Dimensions in mm
A	Reel Outer Diameter	330±1.0
B	Reel Inner Diameter	62±1.5
C	Spindle Hole Diameter	13.0+0.5 −0.2
D	Key Slit Width	2.0±0.5
T1	Space Between Flange	24.8+0.3 −0.2
T2	Reel Thickness	30.2±0.2

Carrier Tape Dimensions



SOP 32W

Symbol	Description	Dimensions in mm
W	Carrier Tape Width	32.0+0.3 −0.1
P	Cavity Pitch	16.0±0.1
E	Perforation Position	1.75±0.1
F	Cavity to Perforation (Width Direction)	14.2±0.1
D	Perforation Diameter	1.55+0.1
D1	Cavity Hole Diameter	2.0+0.25
P0	Perforation Pitch	4.0±0.1
P1	Cavity to Perforation (Length Direction)	2.0±0.1
A0	Cavity Length	14.7±0.1
B0	Cavity Width	20.9±0.1
K1	Cavity Depth	3.0±0.1
K2	Cavity Depth	3.4±0.1
t	Carrier Tape Thickness	0.35±0.05
C	Cover Tape Width	25.5



PLCC 32

Symbol	Description	Dimensions in mm
W	Carrier Tape Width	24.0±0.3
P	Cavity Pitch	18.0±0.1
E	Perforation Position	1.75±0.1
F	Cavity to Perforation (Width Direction)	11.5±0.1
D	Perforation Diameter	1.5+0.1
D1	Cavity Hole Diameter	$1.55^{+1.0}_{-0.05}$
P0	Perforation Pitch	4.0±0.1
P1	Cavity to Perforation (Length Direction)	2.0±0.1
A0	Cavity Length	13.1±0.1
B0	Cavity Width	15.5±0.1
K0	Cavity Depth	3.9±0.1
t	Carrier Tape Thickness	0.30±0.05
C	Cover Tape Width	21.3

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