HT27LC512
CMOS 64K×8-Bit OTP EPROM

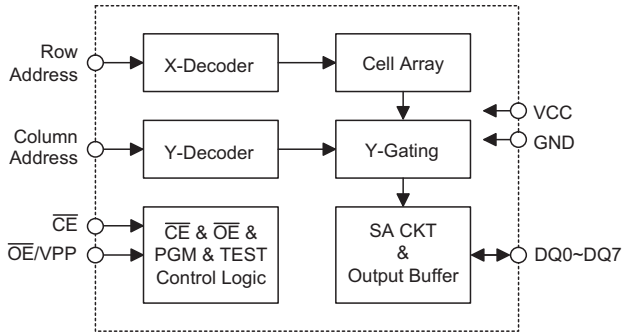
Features

- 64K×8-bit organization
- Single +3.3V power supply
- Programming voltage
  - V_{PP}=12.2V±0.2V
  - V_{CC}=5.8V±0.2V
- Low power consumption
  - Active: 15mA max.
  - Standby: 1μA typ.
- Fast read access time: 120ns
- CMOS and TTL compatible I/O
- Commercial and industrial temperature range
- Fast programming algorithm
- Read access time: 90ns
- Programming time 75μs typ.
- High-reliability CMOS technology
- Latch-up immunity to 100mA from -1.0V to V_{CC}+1.0V
- Two line control ($\overline{OE}$ & $\overline{CE}$)
- Standard product identification code
- Commercial temperature ranges (0°C to +70°C)
- 28-pin DIP/SOP/TSOP, 32-pin PLCC package

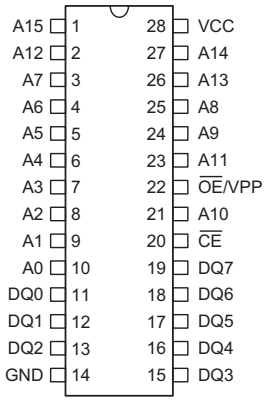
General Description

The HT27LC512 chip family is a low-power, 512K bit, +3.3V electrically one-time programmable (OTP) read-only memories (EPROM). Organized into 64K words with 8 bits per word, it features a fast single address location programming, typically at 75μs per byte. Any byte can be accessed in less than 90ns with respect to Spec. This eliminates the need for WAIT states in high-performance microprocessor systems. The HT27LC512 has separate Output Enable ($\overline{OE}$) and Chip Enable ($\overline{CE}$) controls which eliminate bus contention issues.

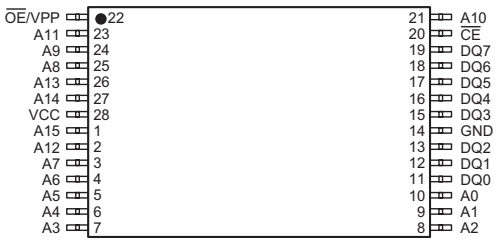
Block Diagram



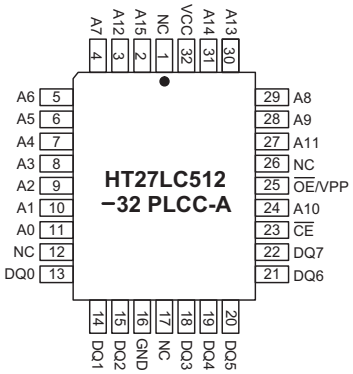
Pin Assignment

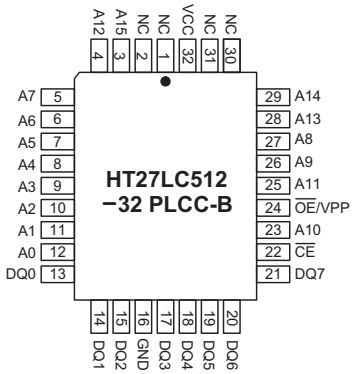


HT27LC512
– 28 DIP-A/SOP-A



HT27LC512
– 28 TSOP-A





Pin Description

Pin Name	I/O/C/P	Description
A0~A15	I	Address inputs
DQ0~DQ7	I/O	Data inputs/outputs
$\overline{CE}$	C	Chip enable
$\overline{OE}$/VPP	C/P	Output enable/program voltage supply
NC	—	No connection

Absolute Maximum Ratings

Operation Temperature Commercial ..... 0°C to +70°C

Storage Temperature ..... –65°C to 125°C

Applied VCC Voltage with Respect to GND ..... 0.6V to 7.0V

Applied Voltage on Input Pin with Respect to GND ..... 0.6V to 7.0V

Applied Voltage on Output Pin with Respect to GND ..... 0.6V to V_{CC}+0.5V

Applied Voltage on A9 Pin with Respect to GND ..... 0.6V to 13.5V

Applied VPP Voltage with Respect to GND ..... 0.6V to 13.5V

Applied READ Voltage (Functionality is guaranteed between these limits) ..... +3V to +3.6V

Note: These are stress ratings only. Stresses exceeding the range specified under. "Absolute Maximum Ratings" may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

D.C. Characteristics

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{CC}	Conditions				
Read Operation							
V_{OH}	Output High Level	3.3V	I_{OH}=–0.4mA	2.4	—	—	V
V_{OL}	Output Low Level	3.3V	I_{OL}=2.0mA	—	—	0.45	V
V_{IH}	Input High Level	3.3V	—	2.0	—	V_{CC}+0.5	V
V_{IL}	Input Low Level	3.3V	—	0.3	—	0.8	V
I_{LI}	Input Leakage Current	3.3V	V_{IN}=0 to 3.6V	5	—	5	μA
I_{LO}	Output Leakage Current	3.3V	V_{OUT}=0 to 3.6V	10	—	10	μA
I_{CC}	VCC Active Current	3.3V	$\overline{CE}$=V_{IL}, f=5MHz, I_{OUT}=0mA	—	—	15	mA
I_{SB1}	Standby Current (CMOS)	3.3V	$\overline{CE}$=V_{CC}±0.3V	—	1.0	10	μA
I_{SB2}	Standby Current (TTL)	3.3V	$\overline{CE}$=V_{IH}	—	—	0.6	mA
I_{PP}	VPP Read/Standby Current	3.3V	$\overline{CE}$=$\overline{OE}$=V_{IL}, V_{PP}=V_{CC}	—	—	100	μA
Programming Operation							
V_{OH}	Output High Level	5.8V	I_{OH}=0.4mA	2.4	—	—	V
V_{OL}	Output Low Level	5.8V	I_{OL}=2.1mA	—	—	0.45	V
V_{IH}	Input High Level	5.8V	—	0.7V_{CC}	—	V_{CC}+0.5	V
V_{IL}	Input Low Level	5.8V	—	–0.5	—	0.8	V
I_{LI}	Input Load Current	5.8V	V_{IN}=V_{IL}, V_{IH}	—	—	5.0	μA
V_H	A9 Product ID Voltage	5.8V	—	11.5	—	12.5	V
I_{CC}	VCC Supply Current	5.8V	—	—	—	40	mA
I_{PP}	VPP Supply Current	5.8V	$\overline{CE}$=V_{IL}	—	—	10	mA
Capacitance							
C_{IN}	Input Capacitance	3.3V	V_{IN}=0V	—	8	12	pF
C_{OUT}	Output Capacitance	3.3V	V_{OUT}=0V	—	8	12	pF
C_{VPP}	VPP Capacitance	3.3V	V_{PP}=0V	—	18	25	pF

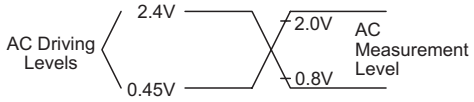
A.C. Characteristics

Ta=+25°C±5°C

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{CC}	Conditions				
Read Operation							
t_{ACC}	Address to Output Delay	3.3V	$\overline{CE}$=$\overline{OE}$=V_{IL}	—	—	90	ns
t_{CE}	Chip Enable to Output Delay	3.3V	$\overline{OE}$=V_{IL}	—	—	90	ns
t_{OE}	Output Enable to Output Delay	3.3V	$\overline{CE}$=V_{IL}	—	—	45	ns
t_{DF}	$\overline{CE}$ or $\overline{OE}$ High to Output Float, Whichever Occurred First	3.3V	—	—	—	40	ns
t_{OH}	Output Hold from Address, $\overline{CE}$ or $\overline{OE}$, Whichever Occurred First	3.3V	—	0	—	—	ns

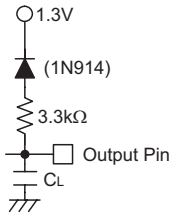
Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{CC}	Conditions				
Programming Operation							
t_{AS}	Address Setup Time	5.8V	—	2	—	—	μs
t_{OES}	$\overline{CE}$/VPP Setup Time	5.8V	—	2	—	—	μs
t_{OEH}	$\overline{OE}$/VPP Hold Time	5.8V	—	2	—	—	μs
t_{DS}	Data Setup Time	5.8V	—	2	—	—	μs
t_{AH}	Address Hold Time	5.8V	—	0	—	—	μs
t_{DH}	Data Hold Time	5.8V	—	2	—	—	μs
t_{DFP}	Output Enable to Output Float Delay	5.8V	—	0	—	130	ns
t_{PW}	PGM Program Pulse Width	5.8V	—	30	75	105	μs
t_{VCS}	VCC Setup Time	5.8V	—	2	—	—	μs
t_{DV}	Data Valid From $\overline{CE}$	5.8V	—	—	—	150	ns
t_{VR}	$\overline{OE}$/VPP Recovery Time	5.8V	—	2	—	—	μs

Test Waveforms and Measurements



t_R, t_F< 20ns (10% to 90%)

Output Test Load



Note: C_L=100pF including jig capacitance

Product Identification Code

Code	Pins										Hex Data
	A0	A1	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	
Manufacturer	0	1	0	0	0	1	1	1	0	0	1C
Device Type	1	1	1	0	0	0	0	0	1	1	83
Continuation	0	0	0	1	1	1	1	1	1	1	7F
	1	0	0	1	1	1	1	1	1	1	7F

Functional Description

Operation Mode

All the operation modes are shown in the table following.

Mode	$\overline{CE}$	$\overline{OE}$/VPP	A0	A9	Output
Read	V_{IL}	V_{IL}	X (2)	X	Dout
Output Disable	V_{IL}	V_{IH}	X	X	High Z
Standby (TTL)	V_{IH}	X	X	X	High Z
Standby (CMOS)	$V_{CC}\pm$ 0.3V	X	X	X	High Z
Program	V_{IL}	V_{PP}	X	X	D_{IN}
Program Verify	V_{IL}	V_{IL}	X	X	D_{OUT}
Product Inhibit	V_{IH}	V_{PP}	X	X	High Z
Manufacturer Code (3)	V_{IL}	V_{IL}	V_{IL}	V_H (1)	1C
Device Code (3)	V_{IL}	V_{IL}	V_{IH}	V_H (1)	83

Note: (1) V_H = 12.0V±0.5V

(2) X=Either V_{IH} or V_{IL}

(3) For Manufacturer Code and Device Code, A1=V_{IH}, When A1=V_{IL}, both codes will read 7F

Programming of the HT27LC512

When the HT27LC512 is delivered, the chip has all 512K bits in the ″ONE″ or HIGH state. ″ZEROs″ are loaded into the HT27LC512 through the procedure of programming.

The programming mode is entered when 12.2±0.2V is applied to the $\overline{OE}$/VPP pin and $\overline{CE}$ is at V_{IL}. For programming, the data to be programmed is applied with 8 bits in parallel to the data pins.

The programming flowchart in Figure 3. shows the fast interactive programming algorithm. The interactive algorithm reduces programming time by using 30μs to 105μs programming pulses and giving each address only as many pulses as is necessary in order to reliably program the data. After each pulse is applied to a given address, the data in that address is verified. If the data is not verified, additional pulses are given until it is verified or until the maximum number of pulses is reached. This process is repeated while sequencing through each address of the HT27LC512. This part of the programming algorithm is carried at V_{CC}=5.8V to assure that each EPROM bit is programmed to a sufficiently high threshold voltage. This ensures that all bits have sufficient margin. After the final address is completed, the entire EPROM memory is read at V_{CC}=V_{PP}=3.3±0.3V to verify the entire memory.

Program Inhibit Mode

Programming of multiple HT27LC512 in parallel with different data is also easily accomplished by using the Program Inhibit Mode. Except for $\overline{CE}$, all like inputs of the parallel HT27LC512 may be common. A TTL low-level program pulse applied to an HT27LC512 $\overline{CE}$ input with $\overline{OE}$/VPP=12.2±0.2V will program that HT27LC512. A high-level $\overline{CE}$ input inhibits the other HT27LC512 from being programmed.

Program Verify Mode

Verification should be performed on the programmed bits to determine whether they were correctly programmed. The verification should be performed with $\overline{OE}$/VPP and $\overline{CE}$ at V_{IL}. Data should be verified at t_{DV} after the falling edge of $\overline{CE}$.

Auto Product Identification

The Auto Product Identification mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by the programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C±5°C ambient temperature range that is required when programming the HT27LC512.

To activate this mode, the programming equipment must force 12.0±0.5V on the address line A9 of the HT27LC512. Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 from V_{IL} to V_{IH}, when A1=V_{IH}. All other address lines must be held at V_{IH} during Auto Product Identification mode.

Byte 0 (A0=V_{IL}) represents the manufacturer code, and byte 1 (A0=V_{IH}), the device code. For HT27LC512, these two identifier bytes are shown in the Mode Select Table. All identifiers for the manufacturer and device codes will possess odd parity, with the MSB (DQ7) defined as the parity bit. When A1=V_{IL}, the HT27LC512 will read out the binary code of 7F, continuation code, to signify the unavailability of manufacturer ID codes.

Read Mode

The HT27LC512 has two control functions, both of which must be logically satisfied in order to obtain data at outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs (t_{OE}) after the falling edge of $\overline{OE}$, assuming the $\overline{CE}$ has been LOW and addresses have been stable for at least t_{ACC}-t_{OE}.

Standby Mode

The HT27LC512 has CMOS standby mode which reduces the maximum VCC current to 10μA. It is placed in CMOS standby when $\overline{CE}$ is at V_{CC}±0.3V. The HT27LC512 also has a TTL-standby mode which reduces the maximum VCC current to 0.6mA. It is placed in TTL-standby when $\overline{CE}$ is at V_{IH}. When in standby mode, the outputs are in a high-impedance state, independent of the $\overline{OE}$ input.

Two-line Output Control Function

To accommodate multiple memory connections, a two-line control function is provided to allow for:

- Low memory power consumption
- Assurance that output bus contention will not occur.

It is recommended that $\overline{CE}$ be decoded and used as the primary device-selection function, while $\overline{OE}$ be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low-power standby mode and that the output pins are only active when data is desired from a particular memory device.

System Considerations

During the switch between active and standby conditions, transient current peaks are produced on the rising and falling edges of Chip Enable. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. At a minimum, a 0.1μF ceramic capacitor (high frequency, low inherent inductance) should be used on each device between VCC and VPP to minimize transient effects. In addition, to overcome the voltage drop caused by the inductive effects of the printed circuit board traces on EPROM arrays, a 4.7μF bulk electrolytic capacitor should be used between VCC and VPP for each eight devices. The location of the capacitor should be close to where the power supply is connected to the array.

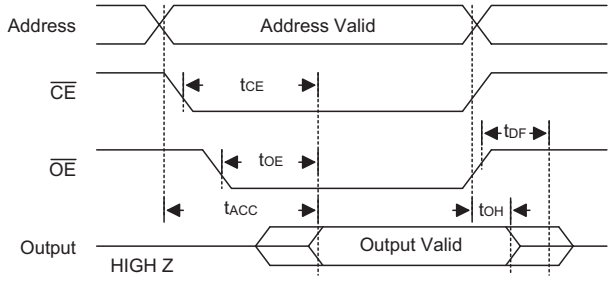


Figure 1. A.C. Waveforms for Read Operation

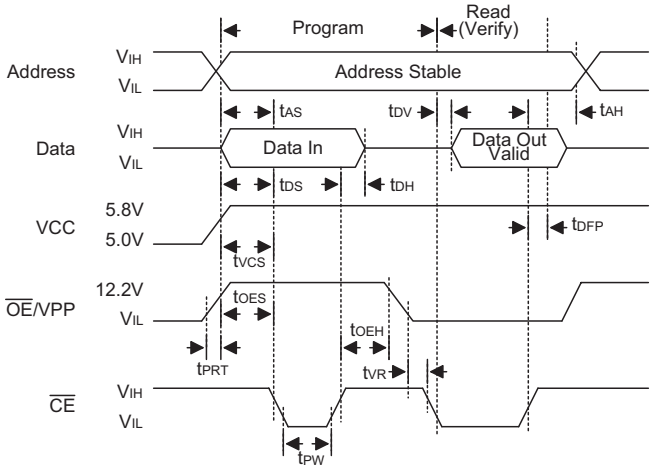
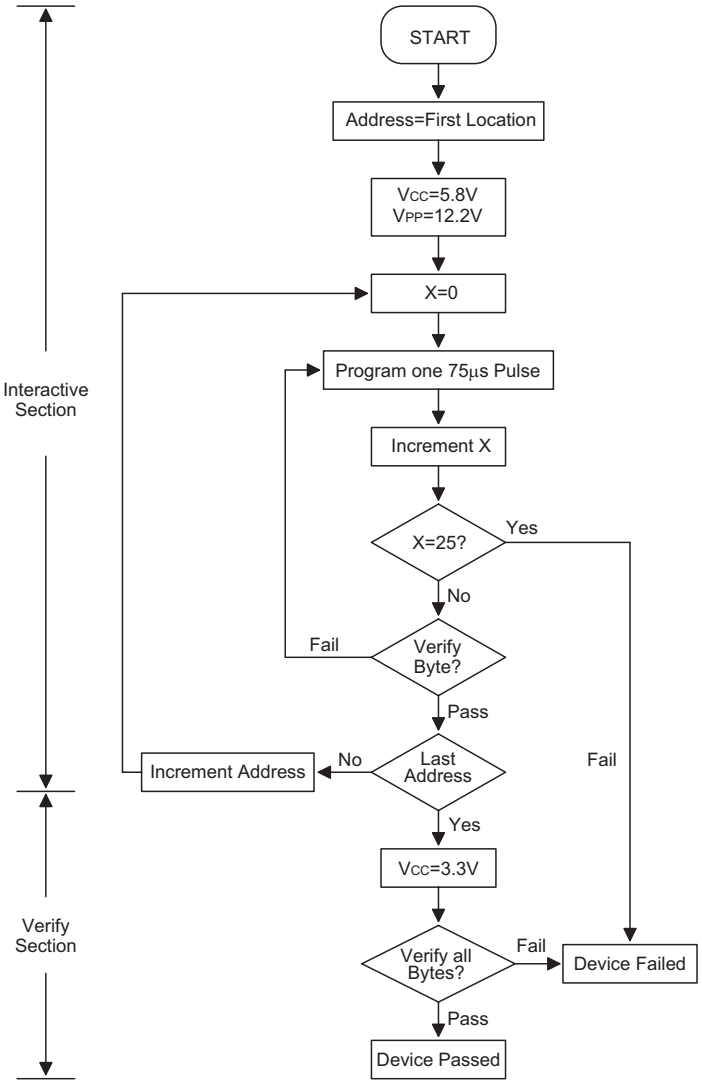


Figure 2. Programming Waveforms

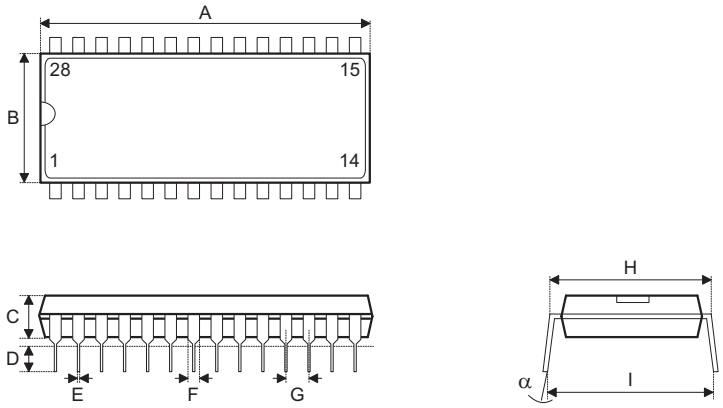


Note: Either 105μs or 30μs pulse.

Figure 3. Fast Programming Flowchart

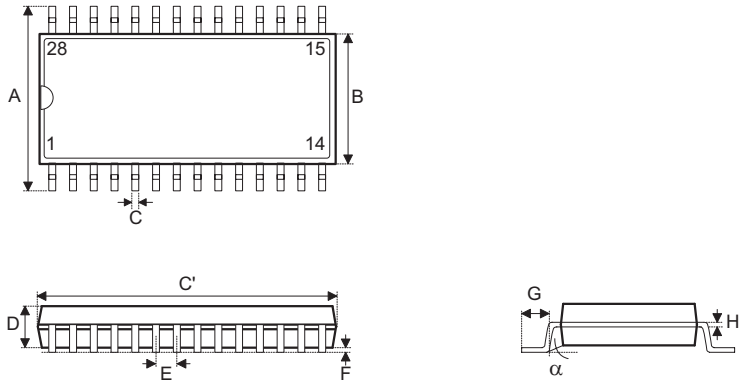
Package Information

28-pin DIP (600mil) Outline Dimensions



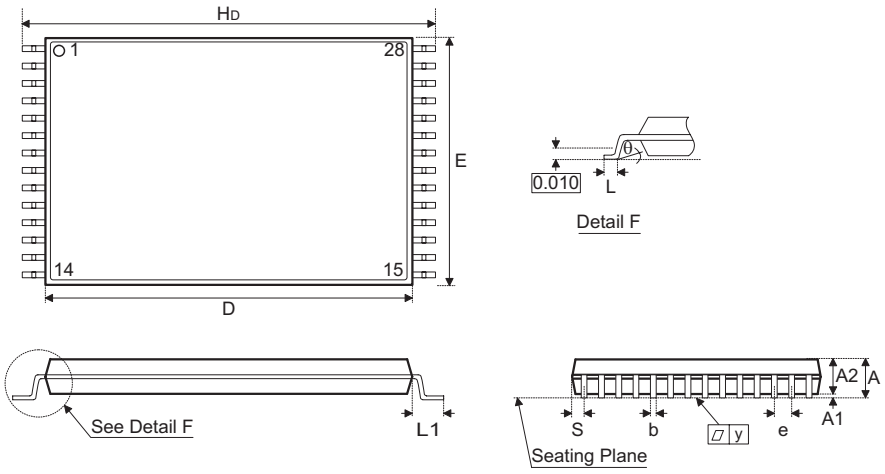
Symbol	Dimensions in mil		
	Min.	Nom.	Max.
A	1445	—	1465
B	535	—	555
C	145	—	155
D	125	—	145
E	16	—	20
F	50	—	70
G	—	100	—
H	595	—	615
I	635	—	670
α	0°	—	15°

28-pin SOP (300mil) Outline Dimensions



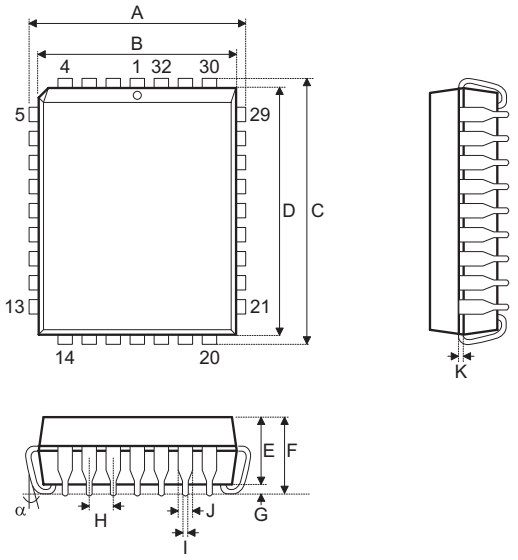
Symbol	Dimensions in mil		
	Min.	Nom.	Max.
A	394	—	419
B	290	—	300
C	14	—	20
C′	697	—	713
D	92	—	104
E	—	50	—
F	4	—	—
G	32	—	38
H	4	—	12
α	0°	—	10°

28-pin TSOP (8×13.4) Outline Dimensions



Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	—	—	1.25
A1	0.08	—	0.18
A2	0.95	—	1.05
b	—	0.20	—
D	11.70	—	11.90
H_D	13.20	—	13.60
E	7.90	—	8.10
e	—	0.55	—
L	—	0.50	—
L1	—	0.8	—
θ	0°	—	5°

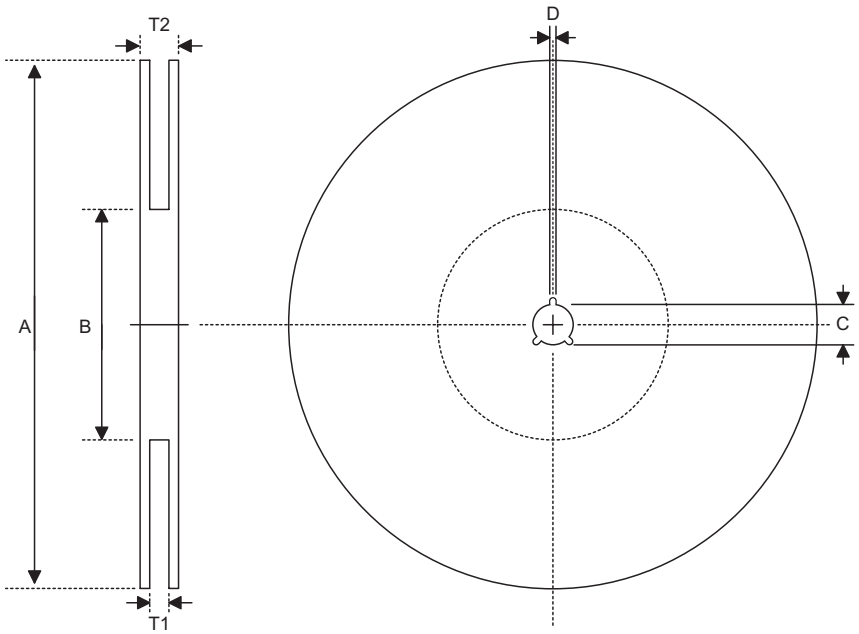
32-pin PLCC Outline Dimensions



Symbol	Dimensions in mil		
	Min.	Nom.	Max.
A	485	—	495
B	445	—	455
C	585	—	595
D	545	—	555
E	105	—	115
F	—	—	140
G	15	—	—
H	—	50	—
I	16	—	22
J	24	—	32
K	8	—	12
α	0°	—	10°

Product Tape and Reel Specifications

Reel Dimensions



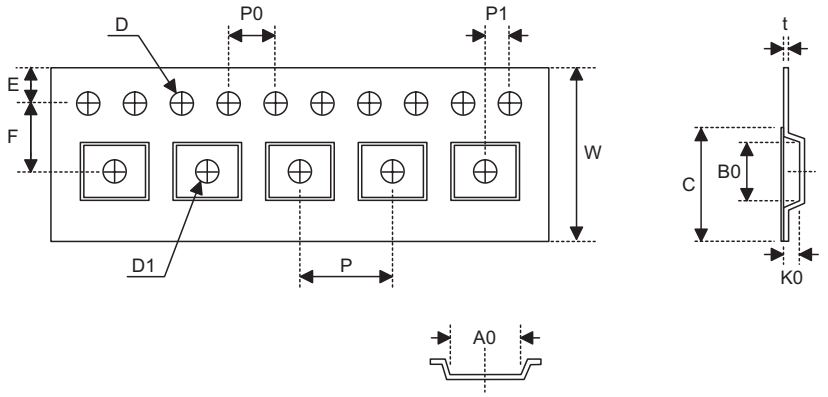
SOP 28W (300mil)

Symbol	Description	Dimensions in mm
A	Reel Outer Diameter	330±1.0
B	Reel Inner Diameter	62±1.5
C	Spindle Hole Diameter	13.0+0.5 −0.2
D	Key Slit Width	2.0±0.5
T1	Space Between Flange	24.8+0.3 −0.2
T2	Reel Thickness	30.2±0.2

PLCC 32

Symbol	Description	Dimensions in mm
A	Reel Outer Diameter	330±1.0
B	Reel Inner Diameter	62±1.5
C	Spindle Hole Diameter	13.0+0.5 −0.2
D	Key Slit Width	2.0±0.5
T1	Space Between Flange	24.8+0.3 −0.2
T2	Reel Thickness	30.2±0.2

Carrier Tape Dimensions



SOP 28W (300mil)

Symbol	Description	Dimensions in mm
W	Carrier Tape Width	24.0±0.3
P	Cavity Pitch	12.0±0.1
E	Perforation Position	1.75±0.1
F	Cavity to Perforation (Width Direction)	11.5±0.1
D	Perforation Diameter	1.5+0.1
D1	Cavity Hole Diameter	1.5+0.25
P0	Perforation Pitch	4.0±0.1
P1	Cavity to Perforation (Length Direction)	2.0±0.1
A0	Cavity Length	10.85±0.1
B0	Cavity Width	18.34±0.1
K0	Cavity Depth	2.97±0.1
t	Carrier Tape Thickness	0.35±0.01
C	Cover Tape Width	21.3

PLCC 32

Symbol	Description	Dimensions in mm
W	Carrier Tape Width	24.0±0.3
P	Cavity Pitch	18.0±0.1
E	Perforation Position	1.75±0.1
F	Cavity to Perforation (Width Direction)	11.5±0.1
D	Perforation Diameter	1.5+0.1
D1	Cavity Hole Diameter	1.55+1.0 −0.05
P0	Perforation Pitch	4.0±0.1
P1	Cavity to Perforation (Length Direction)	2.0±0.1
A0	Cavity Length	13.1±0.1
B0	Cavity Width	15.5±0.1
K0	Cavity Depth	3.9±0.1
t	Carrier Tape Thickness	0.30±0.05
C	Cover Tape Width	21.3

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