

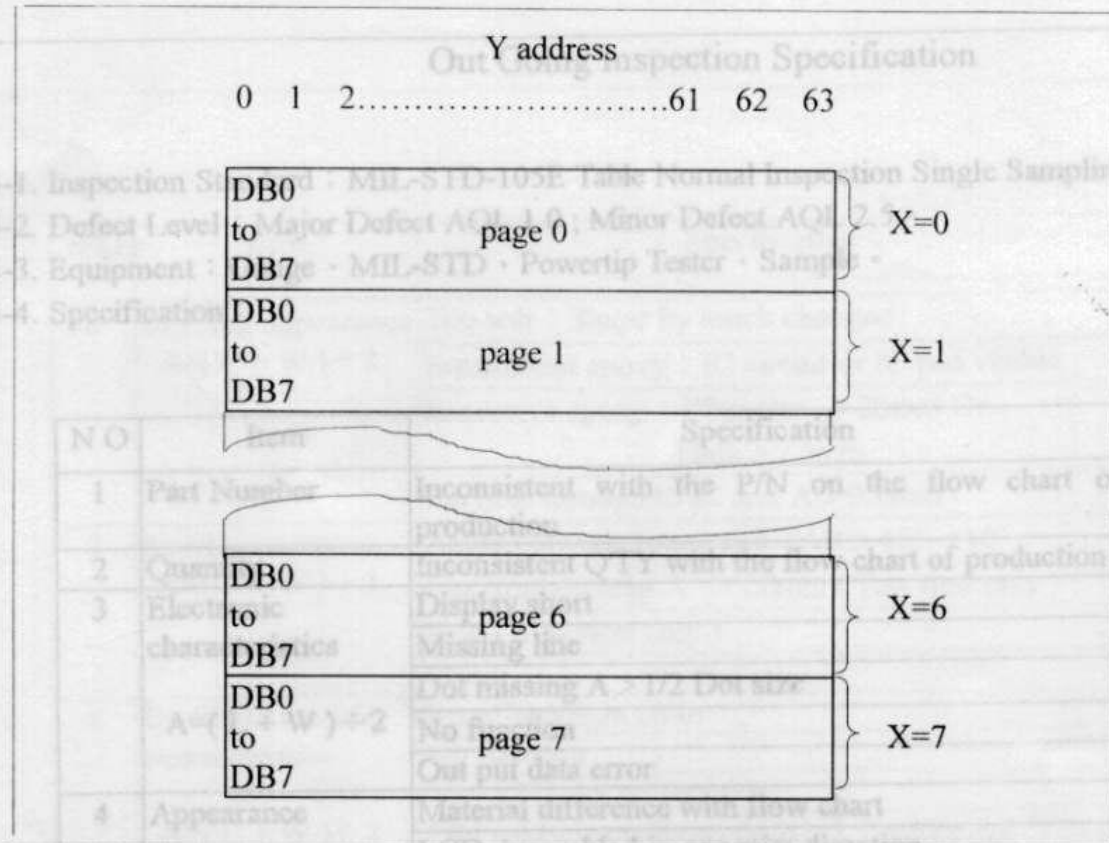


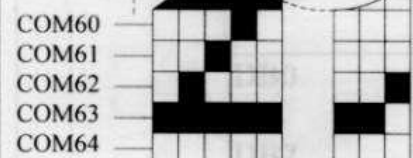
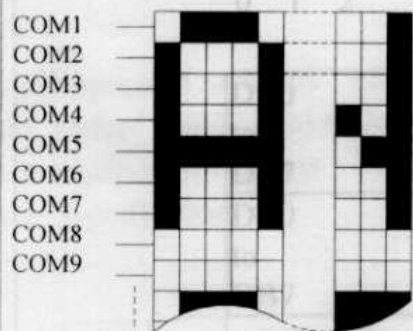
Figure 2 Address Configuration of Display Data RAM

Note: "128*64" consist of 2 "64*64"

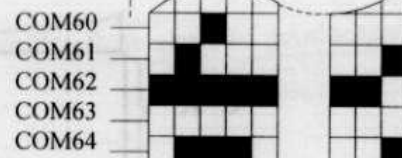
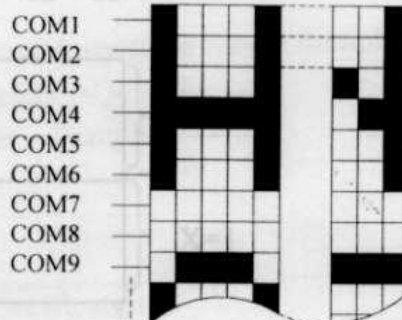
CS1⇒ Chip enable for left 64*64 (segment1 to segment 64)

CS2⇒ Chip enable for right 64*64 (segment 65 to segment 128)

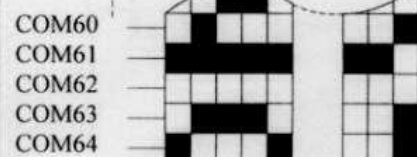
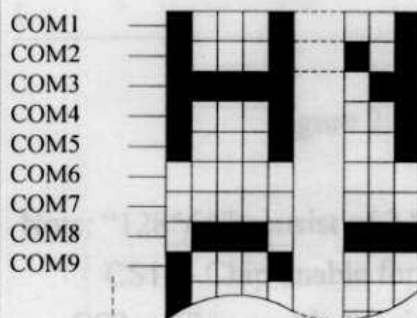




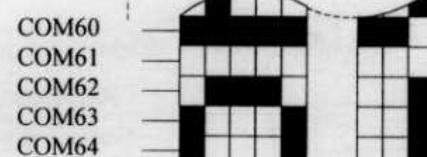
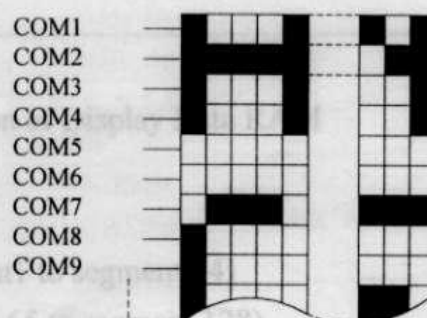
Start line = 0



Start line = 1



Start line = 2



Start line = 3

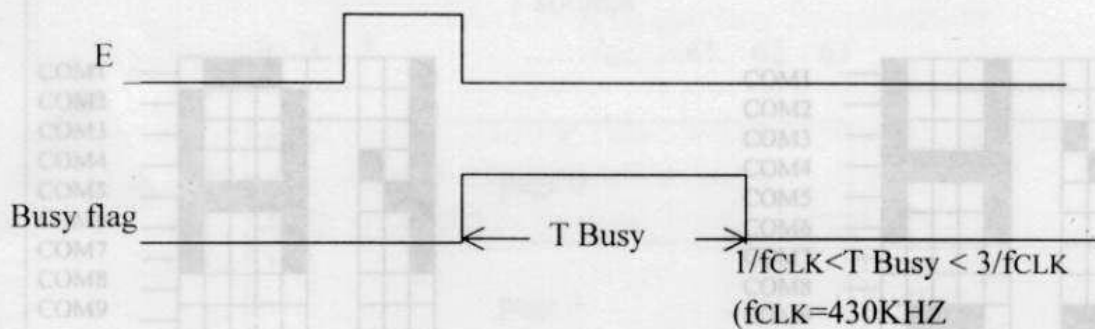
Figure 1 Relation between Start Line and Display



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1, so you should make sure that busy is 0 before writing the next instruction.



- ON/OFF

Shows the liquid crystal display conditions: on condition or off condition.

When on/off is 1, the display is in off condition.

When on/off is 0, the display is in on condition.

- RESET

RESET=1 shows that the system is being initialized. In this condition, no instructions except status read can be accepted.

RESET=0 shows that initializing has finished and the system is in the usual operation condition.

Write Display Data

	R/W D/I		DB7.....DB0						
Code	0	1	D	D	D	D	D	D	D
	MSB			LSB					

Write 8-bit data DDDDDDDD (binary) into the display data RAM. Then Y address is increased by 1 automatically.

Read Display Data

	R/W D/I		DB7..... DB0						
Code	1	1	D	D	D	D	D	D	D
	MSB			LSB					

Reads out 8-bit data DDDDDDDD (binary) from the display data RAM. Then Y address is increased by 1 automatically.

One dummy read is necessary right after the address setting. For details, refer to the explanation of output register in "Function of Each Block".



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Display Start Line

	R/W	D/I	DB7.....DB0						
Code	0	0	1	1	A	A	A	A	A
			MSB				LSB		

Z address AAAAAA (binary) of the display data RAM is set in the display start line register and displayed at the top of the screen. Figure 1 shows examples of display (1/64 duty cycle) when the start line=0-3. When the display duty cycle is 1/64 or more (ex. 1/32, 1/24 etc.), the data of total line number of LCD screen, from the line specified by display start line instruction, is displayed. See figure 1.

Set page (X address)

	R/W	D/I	DB7.....DB0						
Code	0	0	1	0	1	1	1	A	A
			MSB				LSB		

X address AAA (binary) of the display data RAM is set in the X address register. After that, writing or reading to or from MPU is executed in this specified page until the next page is set. See figure 2.

Set Y Address

	R/W	D/I	DB7.....DB0						
Code	0	0	1	D	D	D	D	D	D
			MSB				LSB		

Y address AAAAAA (binary) of the display data RAM is set in the Y address Counter. After that, Y address counter is increased by 1 every time the data is written or read to or from MPU.

Status Read

	R/W	D/I	DB7.....DB0						
Code	1	0	BUSY	0	ON/OFF	REST	0	0	0
			MSB				LSB		

• Busy When busy is 1, the LSI is executing internal operations. No instructions are accepted while busy is



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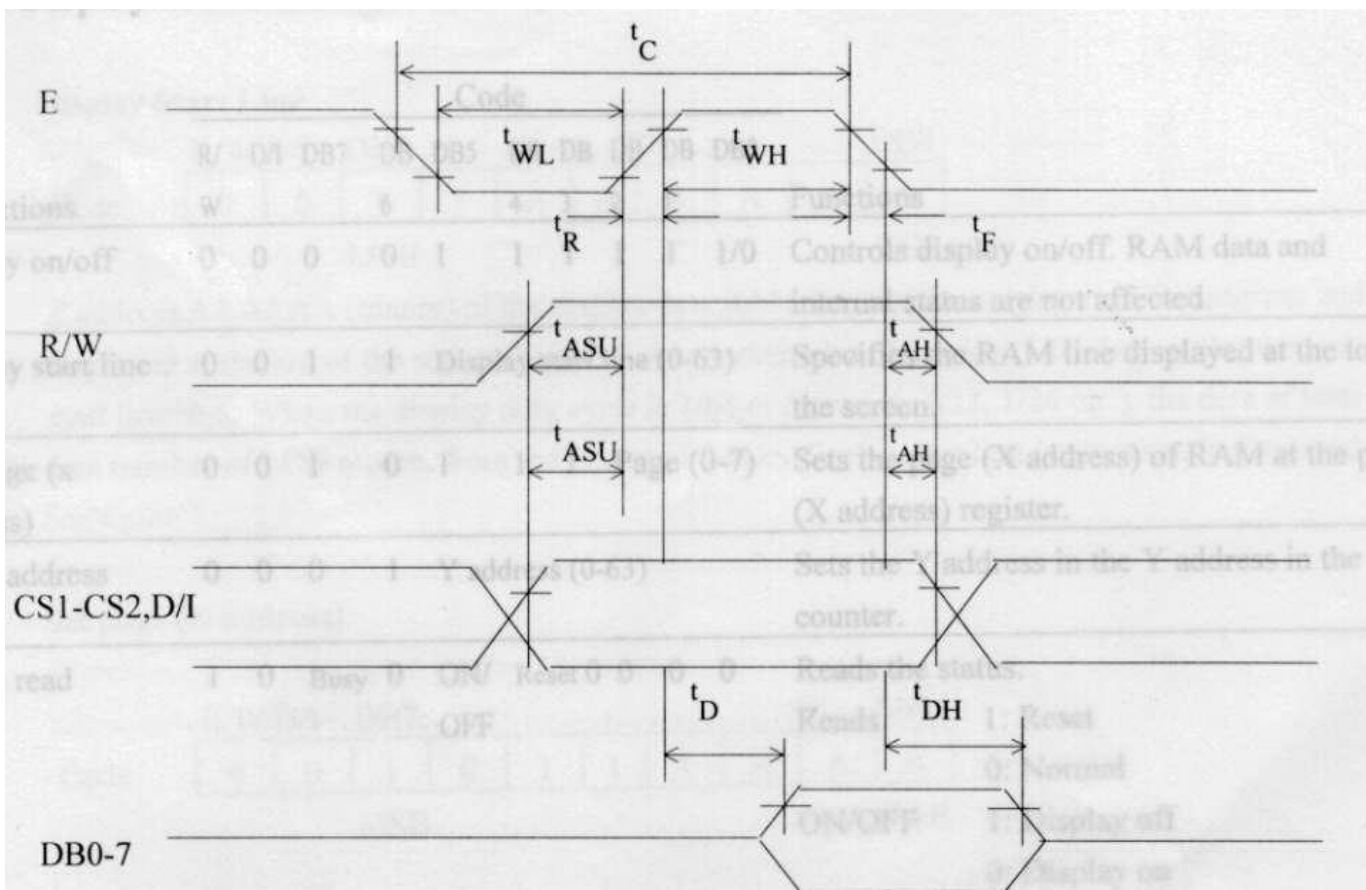
DISPLAY DEVICES FOR BETTER ELECTRONIC DESIGN

Display Start Line			Code									
	R/	D/I	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
on/off	W	0	6	1	4	3	2	1	1	1/0	Functions	
on/off	0	0	0	0	1	1	1	1	1	1/0	Controls display on/off. RAM data and internal status are not affected.	
start line	0	0	1	1	Display start line (0-63)						Specifies the RAM line displayed at the top of the screen.	
Page (X address)	0	0	1	0	1	1	1	Page (0-7)				Sets the page (X address) of RAM at the page (X address) register.
Y address	0	0	0	1	Y address (0-63)							Sets the Y address in the Y address in the counter.
Read	1	0	Busy	0	ON/OFF	Reset	0	0	0	0	Reads the status.	
											Reads	
											1: Reset	
											0: Normal	
											ON/OFF	
											1: Display off	
											0: Display on	
											Busy	
											1: Internal operation	
											0: Ready	
display data	0	1	Write data								Writes data DB0 (LSB) to DB7 (MSB) on the data bus into display RAM.	Has access to the address of the display RAM specified in advance. After the access, Y address is increased by 1.
display data	1	1	Read data								Reads data DB0 (LSB) to DB7 (MSB) from the display RAM to the data bus.	

Display On/Off

	R/W D/I	DB7.....DB0								
Code	0	0	0	0	1	1	1	1	1	D
	MSB									LSB

The display data appears when D is 1 and disappears when D is 0. Though the data is not on the screen with D=0, it remains in the display data RAM. Therefore, you can make it appear by changing D=0 into D=1.



MPU read timing

Characteristic	Symbol	Min.	Typ	Max	Unit
E Cycle	t_C	1000	-	-	ns
E High Level Width	t_{WH}	450	-	-	ns
E Low Level Width	t_{WL}	450	-	-	ns
E Rise Time	t_R	-	-	25	ns
E Fall Time	t_F	-	-	25	ns
Address Set-Up time	t_{ASU}	140	-	-	ns
Address Hold Time	t_{AH}	10	-	-	ns
Data Set-Up Time	t_{SU}	200	-	-	ns
Data Delay Time	t_D	-	-	320	ns
Data Hold Time (Write)	t_{DHW}	10	-	-	ns
Data Hold Time (Read)	t_{DHR}	20	-	-	ns

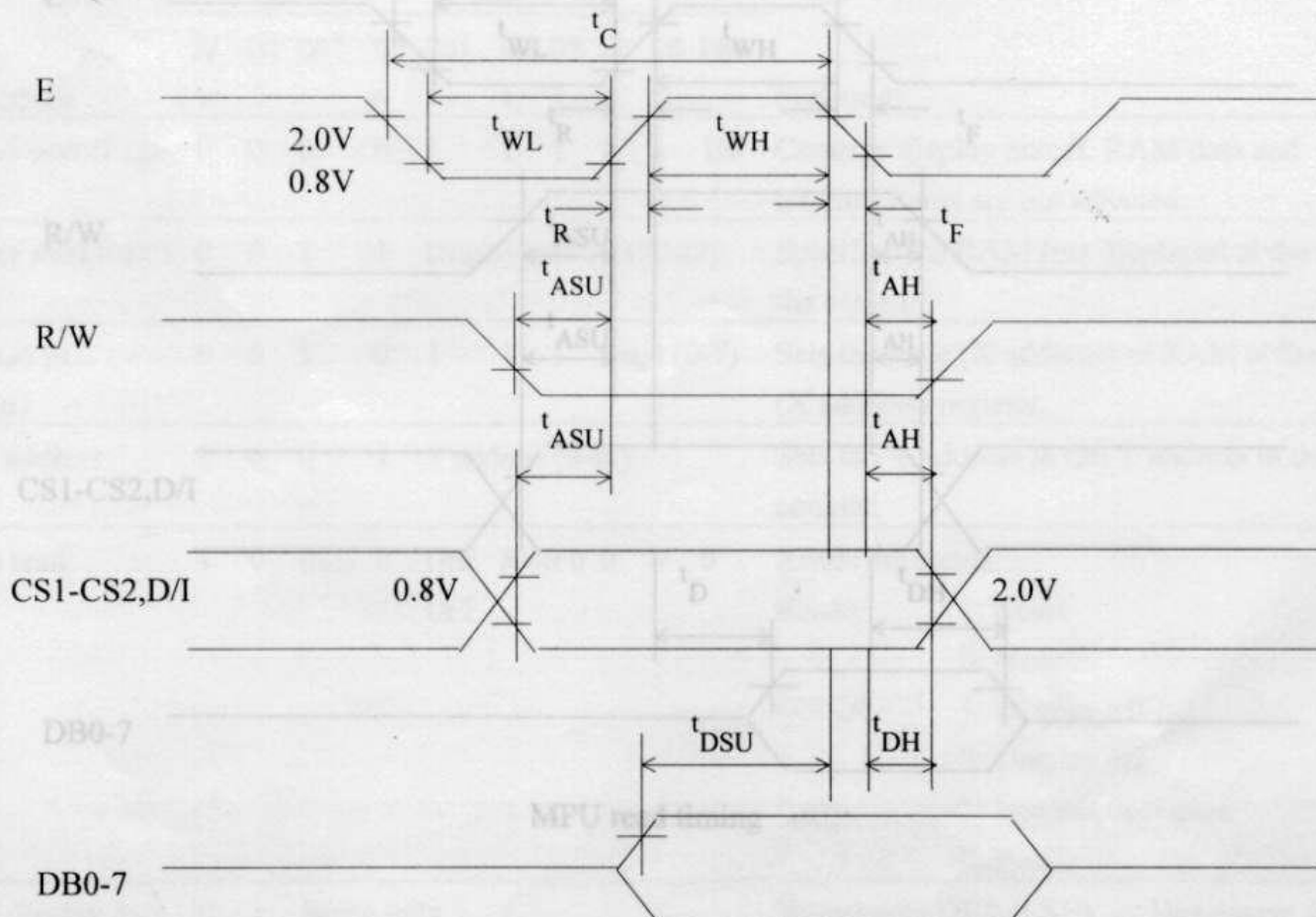
The display data appears when D is 1 and disappears when D is 0. Though the data is not on the screen with D=0, it remains in the display data RAM. Therefore, you can make it appear by changing D=0 into D=1.



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2.3 Timing Characteristics



Characteristic	Symbol	Min.	Typ	Max	Unit
E Cycle	MPU write timing				
E High Level Width	t_{WH}	450	-	-	ns
E Low Level Width	t_{WL}	450	-	-	ns
E Rise Time	t_R	-	-	25	ns
E Fall Time	t_F	-	-	25	ns
Address Set-Up time	t_{ASU}	140	-	-	ns
Address Hold Time	t_{AH}	10	-	-	ns
Data Set-Up Time	t_{DSU}	200	-	-	ns
Data Delay Time	t_D	-	-	320	ns
Data Hold Time (Write)	t_{DHW}	10	-	-	ns
Data Hold Time (Read)	t_{DHR}	20	-	-	ns



MODULE STRUCTURE

2.3 Timing Characteristics

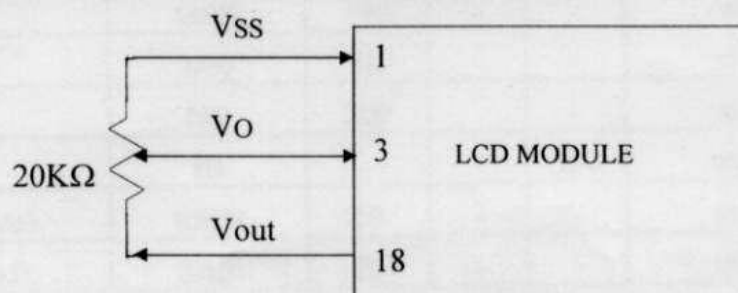
2.1 Counter Drawing

*See Appendix

2.2 Interface Pin Description

Pin No.	Symbol	Function
1	VSS	Signal ground (GND)
2	VDD	Power supply for logic (+5V)
3	Vo	Operating voltage for LCD (variable)
4	D/ $\overline{I}$	Register selection input High =Data register Low =Instruction register (for write) Busy flag address counter (for read)
5	R/ $\overline{W}$	R/W signal input is used to select the read/write mode High =Read mode, Low =Write mode
6	E	Start enable signal to read or write the data
7-10	DB0~ DB3	Four low order bi-directional three-state data bus lines. Use for data transfer between the MPU and the LCD module. These four are not used during 4-bit operation.
11-14	DB4~ DB7	For high order bi-directional three-state data bus lines. Used for data transfer between the MPU and the LCD module. DB7 can be used as a busy flag.
15	CS1	Chip enable for D2 (segment 1 to segment 64)
16	CS2	Chip enable for D3 (segment 65 to segment 128)
17	$\overline{RST}$	Reset signal
18	Vout	Negative voltage power supply
19	A	Power supply for LED backlight (+)
20	K	Power supply for LED backlight (-)

Contrast Adjust



4. Electrical and ambient characteristics: (cont'd)

4.2 Absolute ambient maximum ratings:

Item	Operating		Storage		Comments
	Min.	Max.	Min.	Max.	
Ambient temperature	0 °C	50 °C	-20 °C	60 °C	Note (1)
Humidity	Note (2)		Note (2)		Without condensation
Vibration	---	4.9 m/s ²	---	19.6 m/s ²	XYZ directions
Shock	---	29.4 m/s ²	---	490.0 m/s ²	XYZ directions

Note (1) Ta at 60 °C: 50 hrs Max.

Note (2) Ta ≤ 40°C: 85% RH Max.

Ta > 40 °C : Absolute humidity must be lower than the humidity of 85% at 40°C

4.3 Electrical characteristics: (Ta=25°C Vdd=5.0V ± 0.25V)

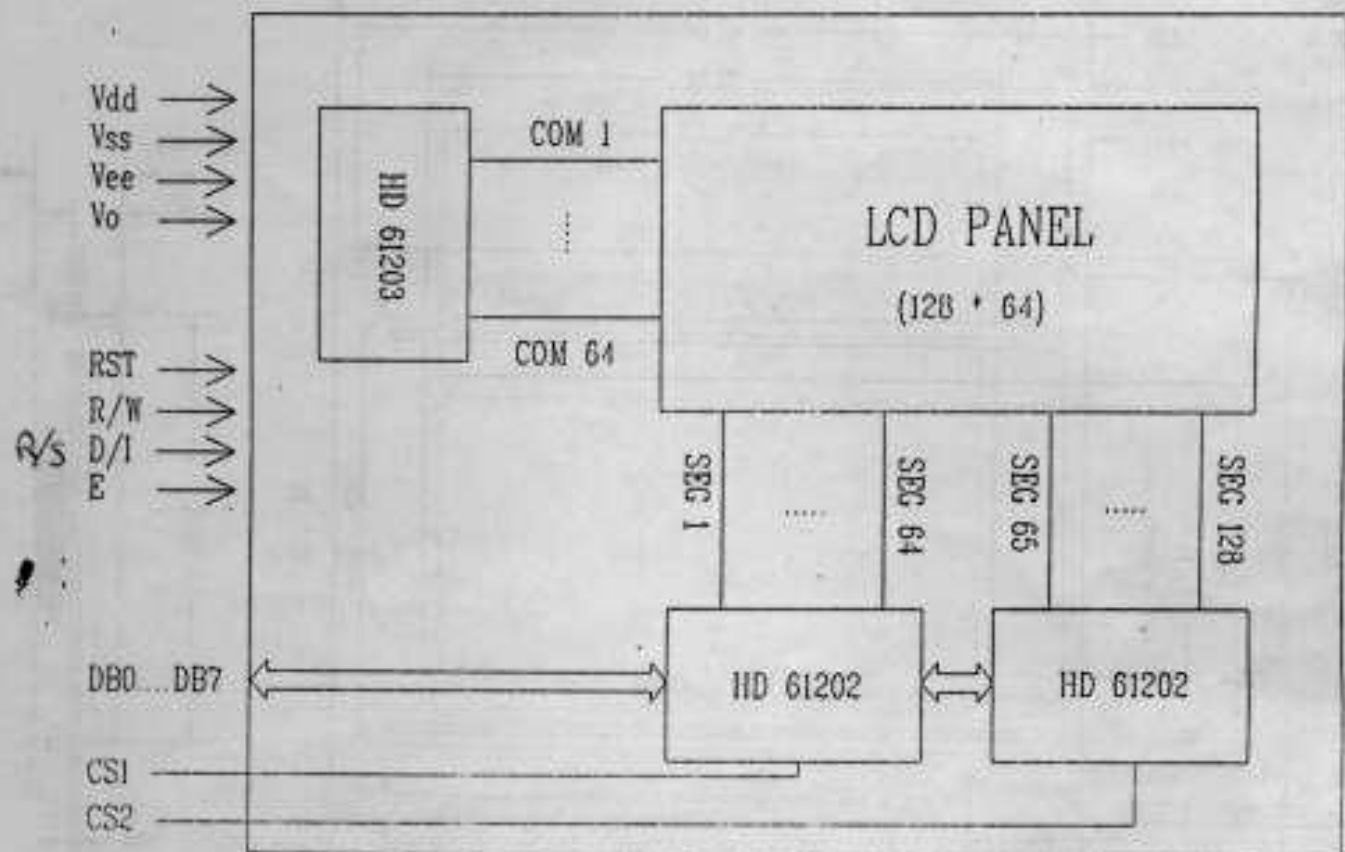
Item	Symbol	Condition	Min.	Typ	Max	Unit
Logic circuit power supply	Vdd-Vss	---	4.5	5.0	5.5	V
LCD driver power supply	Vee-Vss	---	-9.0	-10.0	-11.0	V
Input voltage (High level)	Vih	Note (1)	2.0	---	Vdd	V
Input voltage (Low level)	Vil	Note (1)	0	---	0.8	V
Supply current (Logic)	Idd	Vdd= 5.0 V Vee= -10 V	---	---	4.0	mA
Supply current (LCD)	Ilcd	Vdd= 5.0 V Vee= -10 V	---	---	3.0	mA

Note (1) CS1,CS2,R/W,D/LDB0...DB7,E and RST.

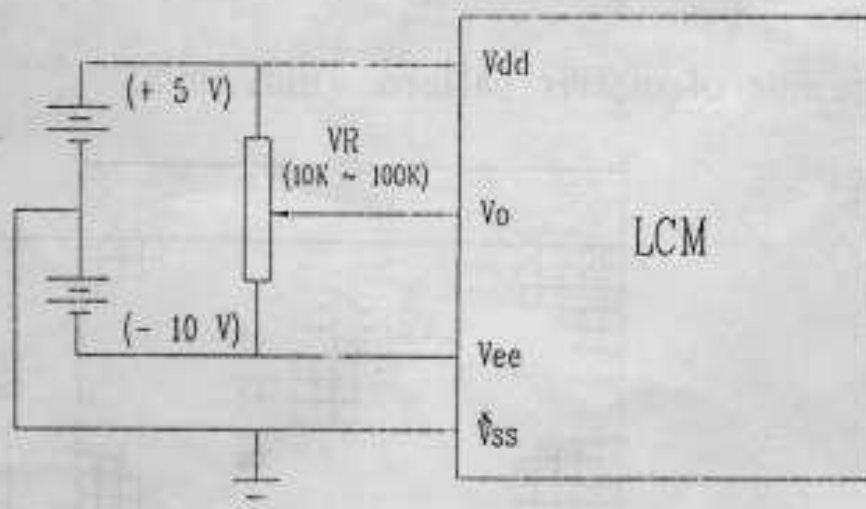
5. Electro-optical characteristics: ($T_a=25\text{ }^{\circ}\text{C}$ $V_{dd}=5\text{ V} \pm 0.25\text{ V}$)

Item	Symbol	Temperature($^{\circ}\text{C}$)	Min.	Typ.	Max.	Unit
Viewing angle	θ	---	---	40 ($K=1.4$)	---	Degree
Contrast ratio	K	---	---	3.0	---	---
Frame frequency	Fr	---	---	70	---	Hz
Response time	T_r (Rise)	0	---	800	---	ms
		25	---	250	---	ms
	T_f (Fall)	0	---	900	---	ms
		25	---	350	---	ms
Operating Voltage	V_{op}	0	13.6	14.0	14.4	V
		25	12.8	13.2	13.6	V
		50	11.6	12.0	12.4	V

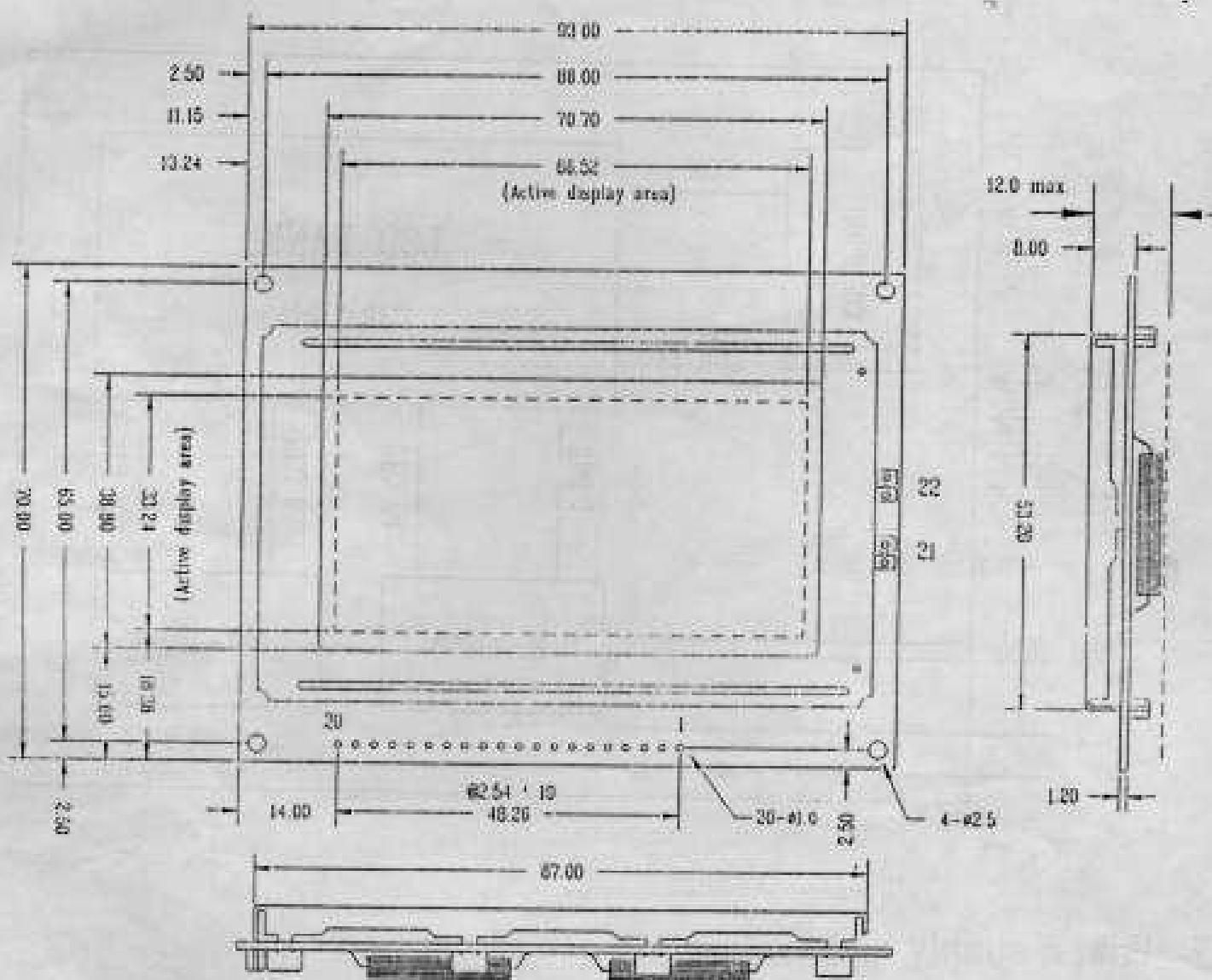
6. Block diagram:



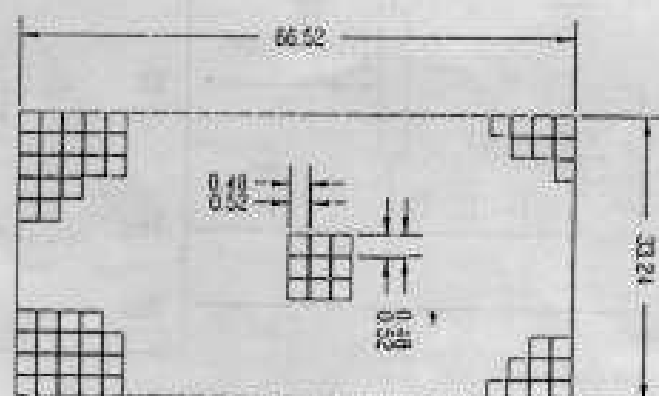
7. Power supply:



8. Outline dimensions (unit: mm)



9. Detail drawing of matrix pattern (unit: mm)



10. Interface pin assignment:

Pin No.	Symbol	Level	Function
1	Vss	---	Ground
2	Vdd	---	Power supply for logic IC (+5 V)
3	V _o	---	Operating voltage for LCD driving
4	D/I	H/L	H: Data input, L: Instruction code input
5	R/W	H/L	H: Data read (ICM --> MPU) L: Data write (ICM <-- MPU)
6	E	H, H --> L	Enable signal
7	DB0	H/L	Data bus three-state I/O common terminal
8	DB1	H/L	Data bus three-state I/O common terminal
9	DB2	H/L	Data bus three-state I/O common terminal
10	DB3	H/L	Data bus three-state I/O common terminal
11	DB4	H/L	Data bus three-state I/O common terminal
12	DB5	H/L	Data bus three-state I/O common terminal
13	DB6	H/L	Data bus three-state I/O common terminal
14	DB7	H/L	Data bus three-state I/O common terminal
15	CS1	H	Chip select for IC1
16	CS2	H	Chip select for IC2
17	RST	L	Reset
18	V _{ee}	---	Power supply for LCD driving circuit
19	N.C.	---	
20	N.C.	---	
21	N.C.	---	
22	N.C.	---	

11. Interface AC characteristics:

(1) MPU Interface

($CND=0V$, $V_{CC}=4.5 \sim 5.5V$, $T_a=-20 \sim +75^{\circ}C$)

Item	Symbol	Min.	Typ.	Max.	Unit	Note
E cycle time	t_{CYC}	1000	-	-	ns	1, 2
E high level width	t_{WEH}	450	-	-	ns	1, 2
E low level width	t_{WEL}	450	-	-	ns	1, 2
E rise time	t_r	-	-	25	ns	1, 2
E fall time	t_f	-	-	25	ns	1, 2
Address setup time	t_{AS}	160	-	-	ns	1, 2
Address hold time	t_{AH}	10	-	-	ns	1, 2
Data setup time	t_{DSW}	200	-	-	ns	1
Data delay time	t_{DDR}	-	-	320	ns	2, 3
Data hold time (Write)	t_{DHW}	10	-	-	ns	1
Data hold time (Read)	t_{DHR}	70	-	-	ns	2

(Note 1)

(Note 2)

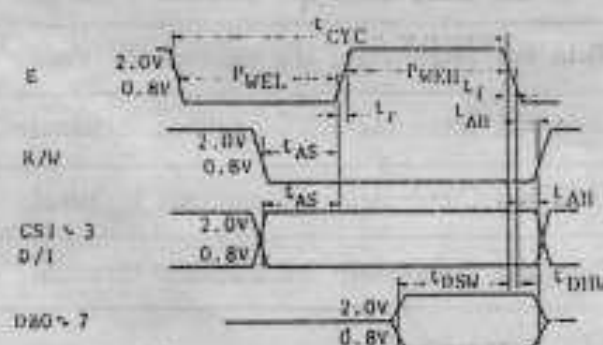


Fig. 1 CPU Write Timing

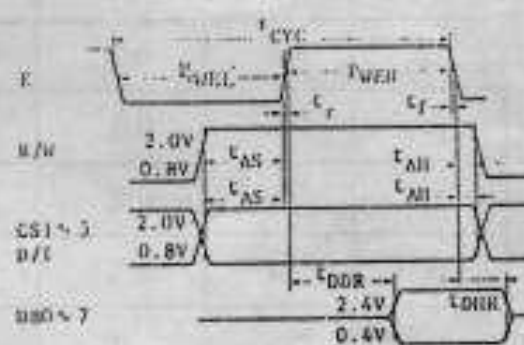
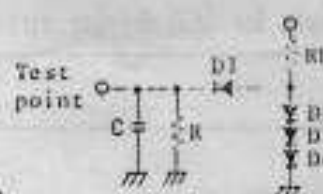


Fig. 2 CPU Read Timing

(Note 3) D00~7 : load circuit



$R1=2.4k\Omega$

$R=11k\Omega$

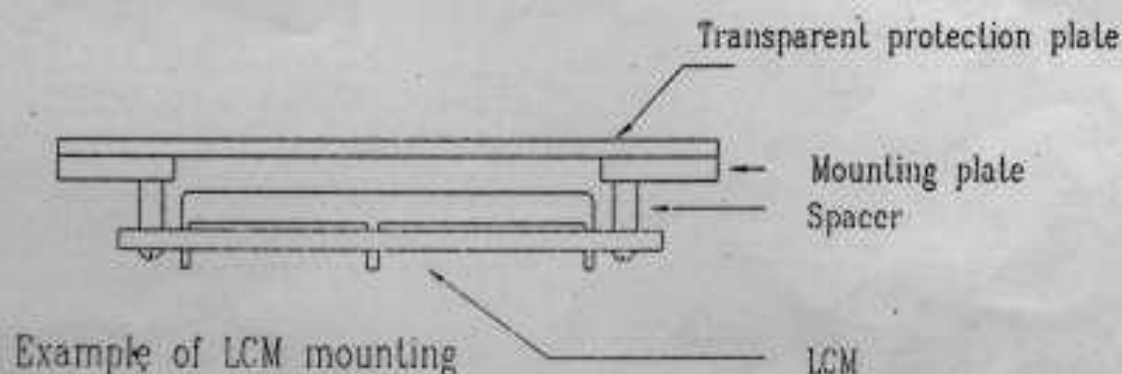
$C=130pF$ (including jig capacity)

Diodes D1 to D4 are all 1S207A(1)

12. Precaution in design and use:

12.1 Mounting method:

Since LCM is constructed as to be fixed by utilizing fitting holes in the Printed Circuit Board as shown below, It is necessary to take consideration of the following items on attachment to a frame.



- (1) Use of a protective plate, which made of acrylic plate, pc ...etc. in order to protect the polarizer and LC cell.
- (2) To prevent the module cover from being pressed, the space between the LCM and the protective plate/mounting plate should be kept 1.0 mm Min.

12.2 Handling precaution:

- (1) Since the liquid crystal cells are made of glass, do not apply strong impact to them.
- (2) If the liquid crystal cell are broken and liquid crystal material touch your body, please wash it off with water as soon as possible.
- (3) The LCM contain C-MOS LSI and protection circuit against static electricity. Do not touch LSI's pins or connector's pins directly. Please earth your body to the ground when you touch them.
- (4) Do not touch the LCD surface to prevent any scratch/contamination to them.