TIMER1 MODULE

Timer1 Module Silicon Errata Sheet

The PICmicro® microcontrollers you have received all exhibit anomalous behavior in their Timer1 modules, as described in this document. They otherwise conform functionally to the descriptions provided in their respective Device Data Sheets and Reference Manuals, as amended by any silicon release errata for particular devices.

Users are encouraged to review the latest Device Data Sheets and errata available for additional information concerning an individual device. These documents may be obtained directly from the Microchip corporate web site, at **www.microchip.com**.

These issues are expected to be resolved in future silicon revisions of the designated parts.

Silicon issue 1 affects all silicon revisions of the following devices:

- PIC16C62A
- PIC16C62B
- PIC16C63
- PIC16C63A
- PIC16C64A
- PIC16C65A
- PIC16C65B
- PIC16C66
- PIC16C67
- PIC16C72
- PIC16C72A
- PIC16C73A
- PIC16C73B
- PIC16C74A
- PIC16C74B
- PIC16C76
- PIC16C77
- PIC16C745
- PIC16C765
- PIC16C773
- PIC16C774
- PIC16C923
- PIC16C924
- PIC16C925
- PIC16C926
- PIC16F72
- PIC16F73
- PIC16F74
- PIC16F76
- PIC16F77
- PIC16F87
- PIC16F88
- PIC16F627A
- PIC16F628A
- PIC16F648A
- PIC16F737
- PIC16F747
- PIC16F767
- PIC16F777
- PIC16F818
- PIC16F819
- PIC16F870
- PIC16F871
- PIC16F872
- PIC16F873
- PIC16F873A
- PIC16F874
- PIC16F874A
- PIC16F876
- PIC16F876A
- PIC16F877
- PIC16F877A
- PIC16F913
- PIC16F914
- PIC16F916
- PIC16F917
- PIC17C42A
- PIC17C43
- PIC17C44
- PIC17C752
- PIC17C756
- PIC17C756A
- PIC17C762
- PIC17C766
- PIC18C242
- PIC18C252
- PIC18C442
- PIC18C452
- PIC18C601
- PIC18C658
- PIC18C801
- PIC18C858
- PIC18F242
- PIC18F248
- PIC18F252
- PIC18F258
- PIC18F442
- PIC18F452
- PIC18F458
- PIC18F1220
- PIC18F1320
- PIC18F2220
- PIC18F2320
- PIC18F2331
- PIC18F2431
- PIC18F2439
- PIC18F2539
- PIC18F4220
- PIC18F4320
- PIC18F4331
- PIC18F4431
- PIC18F4439
- PIC18F4539
- PIC18F6520
- PIC18F6525
- PIC18F6585
- PIC18F6620
- PIC18F6621
- PIC18F6680
- PIC18F6720
- PIC18F8520
- PIC18F8525
- PIC18F8585
- PIC18F8620
- PIC18F8621
- PIC18F8680
- PIC18F8720

TIMER1 MODULE

1. Module: Timer1 (Asynchronous Counter)

When writing to the TMR1H register, under specific conditions, it is possible that the TMR1L register will miss a count while connected to the external oscillator via the T1OSO and T1OSI pins.

When Timer1 is started, the circuitry looks for a falling edge before a rising edge can increment the counter. Writing to the TMR1H register is similar to starting Timer1; therefore, the former logic stated applies any time the TMR1H register is written. If the TMR1H register is not completely written to during the high pulse of the external clock, then the TMR1L register will miss a count due to the circuit operation stated previously. The high pulse of a 32.768 kHz external clock crystal yields a 15.25 μs window for the write to TMR1H to occur. The amount of instructions that can be executed within this window is frequency dependent, as shown in Table 1 below.

TABLE 1: FREQUENCY DEPENDENT INSTRUCTION EXECUTION AMOUNTS

FOSC	TCY (μs)	TCY within 15.25 μs
1 MHz	4	3.81
2 MHz	2	7.63
4 MHz	1	15.25
8 MHz	0.5	30.5
16 MHz	0.25	61
20 MHz	0.2	76.25
40 MHz (PIC18)	0.1	152.5

Work around

Operating Conditions: FOSC ≥ 4 MHz, no wake-ups from Sleep, Timer1 interrupt enabled, global interrupts enabled.

The code excerpts in Example 1, Example 2 and Example 3 show how the TMR1H register can be updated while the external clock (32.768 kHz) is still on its high pulse.

The importance of the code examples is that the **bold** instructions are executed within the first 15.25 μs high pulse on the external clock after the Timer1 overflow occurred. This will allow the TMR1L register to increment correctly.

EXAMPLE 1: PIC16 INTERRUPT SERVICE ROUTINE

```
ISR @ 0x004                         ; (3-4Tcy), fixed interrupt latency

    MOVWF   w_temp                  ; (1Tcy), save off current W register contents
    MOVF    STATUS,w                ; (1Tcy), move status register into W register
    MOVWF   status_temp             ; (1Tcy), save off contents of STATUS register

    BANKSEL PIR                     ; (2Tcy), choose correct SFR bank
    BTFSS   PIR,TMRIF               ; (2Tcy), did a Timer1 overflow occur?
    GOTO    EXIT                    ; No

RELOAD
    BSF     TMR1H,7                 ; (1Tcy) Yes, reload for a 1 second overflow

EXIT
    MOVF    status_temp,w           ; retrieve copy of STATUS register
    MOVWF   STATUS                  ; restore pre-isr STATUS register contents
    SWAPF   w_temp,f
    SWAPF   w_temp,w                ; restore pre-isr W register contents
    RETFIE
                                    Total = 11-12 TCY (if Timer1 overflow occurred)
```

EXAMPLE 2: PIC18 HIGH PRIORITY INTERRUPT SERVICE ROUTINE

```
ISR @ 0x0008                        ; (3-4Tcy), fixed interrupt latency

    BRA     HIGHINT                 ; (2Tcy), go to high priority interrupt routine

HIGHINT
    BTFSC   PIR,TMRIF               ; (1Tcy), did a Timer1 overflow occur?
    BSF     TMR1H,7                 ; (1Tcy) Yes, reload for a 1 second overflow

    RETFIE  FAST
                                    Total  = 7-8 TCY (if Timer1 overflow occurred)
```

EXAMPLE 3: PIC18 LOW PRIORITY INTERRUPT SERVICE ROUTINE

```
ISR @ 0x0018                        ; (3-4Tcy), fixed interrupt latency

    MOVFF   STATUS,STATUS_TEMP      ; (2Tcy), save STATUS register
    MOVFF   WREG,WREG_TEMP          ; (2Tcy), save working register, refer to note 1
    MOVFF   BSR,BSR_TEMP            ; (2Tcy), save BSR register, refer to note 1

    BTFSS   PIR,TMRIF               ; (2Tcy), did a Timer1 overflow occur?
    BRA     EXIT                    ; No
RELOAD
    BSF     TMR1H,7                 ; (1Tcy) Yes, reload for a 1 second overflow

EXIT
    MOVFF   BSR_TEMP,BSR            ;restore BSR register, refer to note 1
    MOVFF   WREG_TEMP,WREG          ;restore working register, refer to note 1
    MOVFF   STATUS_TEMP,STATUS      ;restore STATUS register
    RETFIE

                                    Total  = 12-13 TCY (if Timer1 overflow occurred)
```

Note: These instructions are required based on the function of the ISR. If the only code in the ISR is to reload Timer1, then they are not required, but may be required if additional code is added.

REVISION HISTORY

Revision A Document (4/2005):

Original version of this document. Silicon issue 1 (Timer1 – Asynchronous Counter).

Revision B Document (9/2005):

Updated the list of affected devices.

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