Integrated RF Subsystem and Circuit Design for Short-Range Radio

Part 3 of this series addresses some example subsystem and circuit design issues of Short-Range Radio, particularly from the perspective of designing and using integrated PLL transmitters that are becoming popular replacements for SAW based transmitters. The low power and cost of these systems requires fundamental attention to design detail, which is not an easy task for the often inexperienced designer of these systems operating in a standards vacuum. This task is eased and risk is lowered by basic analysis and use of modern integrated solutions.

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It has been the aim of this series to begin the process of applying the large body of available wireless knowledge to the short-range radio design problem, with a particular emphasis on supporting the less experienced designer. Part 1 of this series introduced top level system design issues such as statistical link budgeting, and Part 2 covered the applicable U.S. and European short-range radio regulations and their impact on system design. Armed with this knowledge we are ready to tackle some of the hardware design issues involved, which despite the apparent simplicity of the product can be quite challenging. Basic theory will be covered in this part, emphasizing the problems and trade-offs faced by the integrated circuit designer and by the board level RF designer. This series will conclude with more design examples and laboratory results in the final Part 4.

A design team developing a product that fits into an accepted industry standard such as cellular in some ways has an easier task than the designer of a short-range radio system. The cellular product is more

complex and is tested to more rigorous and much harder to meet standards, but the standards are documented in great detail and there is no mystery as to the specifications. The designers are seasoned professionals who can draw on the experience and understanding of colleagues and management with years or decades of experience. On the other hand, short-range RFIC designers may have solid IC design experience but limited training in RF design. At the product/board design level, the often inexperienced short-range radio designer is usually handed an edict to just come out with a product that "works" by a certain date, and that can be built for just a few dollars. The companies that build short-range radio products are often experimenting with a new sideline, and the new designer may have no mentors or



managers who have ever designed a radio themselves, and who are not sympathetic to the problems encountered. There is also a very limited supply of short-range radio specific reference material. Combined with these problems is the fact that the designer has complete freedom of action. There is no "standard" to follow, just plenty of rope to hang oneself with while whipping out a new system and circuit design with *very* limited time, money, and guidance! Accepting the fact that successful short-range radio product design can be a significant challenge at the IC and system level, let us turn our attention to how such systems are physically implemented. These issues cannot be covered in depth in a short article, but several key fundamentals can be covered. The references given can take the interested reader to greater depth, and the Microchip web site will be featuring numerous detailed short-range radio application notes as well.

The lowest cost option for short-range radio equipment are the classic LC based links. These are usable in the U.S. and other FCC based countries, but not for Europe with its much tighter frequency accuracy specifications. The lowest cost systems that can generally meet the European requirements are SAW based links. The better frequency accuracy of SAWs over LC allows narrower bandwidth receivers with improved sensitivity and interference immunity. This improved performance with good cost efficiency has led to SAWs being the method of choice over the last decade in wireless keyless entry. However, within the last few years integrated circuit PLL based systems have challenged SAWs on cost effectiveness while providing an improvement in performance over SAWs as significant as the improvement in SAWs was over LC based systems. This improvement is again partly based on better frequency accuracy allowing narrower band and thus improved receivers. However, use of frequency synthesis allows software controlled frequency agility also. The introduction of processors into the links allows error control, transmit power level control, microcellular handoff, and a host of other "big system" type features. These improvements allow reaching up from classic control and security operation into a new world of data communications applications. This opportunity has prompted Microchip Technology and other companies to enter the short-range radio market as suppliers of integrated subsystem solutions. Though lack of standards is still holding back business development, these larger suppliers will by necessity promote standardization that will greatly improve the ability of smaller companies to implement these systems. For example, the Microchip rfPIC12C509 is a PLL ASK (18 pin SOIC 509AG version) and FSK (20 pin SSOP 509AF version) transmitter with integrated PICmicro® controller that is typical of this class of transmitter. Issues such as acceptable phase noise performance, carrier frequency accuracy, and transmitted harmonic suppression are solved by using such a solution with its recommended board level implementation. Its block diagram is shown in Fig. 1. The 20 pin version in the smaller SSOP package has the necessary switch pinned out to do FSK via crystal pulling. The 18 pin SOIC version is primarily intended for ASK modulation, but can use a PICmicro pin as a switch to do FSK.

Current Pump PLL Design

The design of PLLs is in general an involved field, to which entire books are devoted (refs. 4, 5, 6). However, most references do not provide coverage of the most popular "current pump" form of PLL, instead focusing on the older active (op amp based) loop filter forms (ref. 5 excepted). The advantages of the current pump form include not only saving an op amp, but also lower phase noise due to the fact that the current pump is on only a tiny fraction of the time in the locked state, thus greatly reducing flicker noise on the controlling input to the VCO, and thus limiting induced phase noise. Some short-range transmitters have the loop filter on the die and the customer is relieved of the need to understand and design PLLs. Others, such as that on the rfPIC12C509, provide more flexibility by using an off die loop filter that the customer can either design or take from an applications note. Of course, the RFIC designer must have a thorough understanding of the subject.

Since they are not commonly available, design equations for current pump PLLs are given here. They may be developed by applying standard control system frequency domain analysis, and the same basic methods will be used later in analyzing closed loop noise. In applying this type of analysis to PLLs, the variations of voltage, frequency, and phase in the frequency domain as small signal variable around an operating point (the locked frequency). It may seem odd reader to view to the



frequency and phase variations in the frequency domain, but it is perfectly valid. In this analysis the VCO is viewed as an integrator of input voltage to output phase. This is also initially confusing, but it follows directly from the definition of radian frequency being the time derivative of phase. With these points in mind, the system is examined as a feedback control system, which remains stable if the phase shift around the total loop is less than 360 degrees at all frequencies where the loop gain is greater than one. It is also common for the simple analysis of PLLs to be put into what is called "second order normalized form". In this standard form loop parameters may be more easily viewed and understood, and loop component values calculated from the desired loop parameters. The loop parameter of interest are the "natural frequency" ω_n and the "damping factor" ξ . The natural frequency is the frequency at which the loop "rings" when settling. Though related to open loop unity gain bandwidth, the two terms are not the same. The damping factor gives a measure of phase margin and stability. The loop is stable if $\xi > 0$, and it has the fastest settling time if $\xi = 0.707$. It does not noticeably ring if $\xi > 1$, but it does overshoot on step inputs since phase margin is always less than 90 degrees. Since extra filtering with additional phase shift is common in PLLs (this makes them higher than second order and thus not amenable to standard normalized form), a common design practice is to set $\xi = 1.0 - 1.5$ for hand calculation, and then adjust components in simulation to optimize phase margin, settling time, and spurious suppression. A simplified but usefully accurate SPICE model for higher order PLL simulation will be shown for making these simulations.

Referring to **Fig. 2**, the block diagram of an ideal second order current pump PLL is shown (for now ignore the noise voltages V_{nvo} and V_{nvc} which apply to later noise analysis). It is ideal in that the sampling nature of the loop will be ignored, and the analysis performed using continuous variables. This is valid so long as loop bandwidth is a very small fraction of sample rate, but detailed simulation to determine actual phase shift is required when loop bandwidths are a significant (greater than a few percent) fraction of sample rate (reference frequency at the phase detector input). The loop can maintain good stability with a loop bandwidth up to about 10% of the sample rate, though 5% is a safer number. The loop consist of the following components or subsystems:

Reference Frequency Source: The reference is almost always a crystal controlled oscillator, which may be followed by an optional fixed or programmable divider of value "M". The purpose of the PLL is to force the voltage controlled oscillator frequency to be some exact multiple of the reference frequency, thus transferring the high accuracy and quality of the crystal controlled oscillator to a frequency above that at which crystals may directly operate.

Voltage Controlled Oscillator (VCO): This block converts an input "steering" or "tuning" voltage into an output frequency and phase. The VCO on the rfPIC12C509 is a relaxation oscillator, as opposed to the higher Q and quality LC or other resonant oscillators common in standard radios. The high loop bandwidth allowed by the fixed divider and high reference frequency suppress the "phase noise" of the low quality free running relaxation oscillator, thus allowing the use of a limited performance completely integrated VCO. The "gain" of the VCO is normally referred to as K_o and for PLL design normally has units of radians per second per volt (but often used in Hz/V form in noise calculations). Since the analysis is of phase variation and the VCO integrates input voltage to output phase (frequency offset from desired lock "integrates" into a phase error), the control system frequency domain transfer function of the VCO is Ko/s. Like most VCOs, the VCO in the rfPIC12C509 does not show perfect "linearity". It varies over frequency as shown in Table 1, and this variation must be taken into account in design of the PLL to ensure desired loop parameters are achieved while stability and noise performance are maintained.

Frequency			
 (MHZ)	(WHZ/V)		
310	225		
320	253		
330	275		
340	291		
350	306		
360	319		
370	323		
380	323		
390	313		
400	294		
410	274		
420	244		
430	211		
440	177.5		
450	144.6		
460	113.2		
470	78.9		

Table 1. rfPIC12C509 VCO Tune Curve

Frequency Divider: The digital frequency divider

simply divides down the VCO frequency to match the reference frequency. In a frequency agile synthesizer this would be a programmable element. The divider reduces both frequency and phase by its transfer function 1/N.

Phase Detector (PD): The phase detector is almost always a digital subsystem that compares a reference frequency to the divided VCO output, producing a pulse width equal to the time difference between these signals. In the locked state there is no phase difference, so this width approaches zero. In the case of an active loop filter the phase detector output voltage directly drives the loop filter. For the current pump case the phase detector output turns transistor current sources on and off. These current pumps are then actually part of the phase detector, so that the current pump PD output is in current per radian of phase error input. It is a sampled encoding but happens so fast that continuous approximation is valid for basic analysis. The PD will provide a current Ipd for a time representative of up to 2π radians of phase error before the PD "rolls over" (runs out of encoding range by infringing into the next sample time). Its "gain" is therefore $K_d = Ipd/2\pi$ amps/radian.

Loop Filter (LF): The loop filter takes the current pump output currents and via filtering suppresses their high frequency content at the sampling rate and simultaneously converts the current back into a voltage to drive the VCO. A difference in the analysis of current pump vs. op amp active loop filter PLLs is that the active loop filter is a voltage to voltage transfer function, and the current pump form is a current to voltage transfer function. The transfer function is simply the impedance of the loop filter, so since it is in its simplest form a series RC circuit in parallel with the PD output, its transfer function is F(s) = (sRC + 1)/sC.

The phase transfer function of the loop is defined here as:

$$H(s) = \frac{\theta_{out} / N}{\theta_{ref}}$$
(19)

H(s) is the transfer function from the reference input on the phase detector to the feedback input. This will turn out to be a low pass function, and one that is highly indicative of loop locking, tracking, and noise behavior. From Fig. 2 above, if we solve for this relationship we obtain:

$$H(s) = \frac{\frac{K_0 I_{pd} R}{2\pi N} s + \frac{K_0 I_{pd}}{2\pi NC}}{s^2 + \frac{K_0 I_{pd} R}{2\pi N} s + \frac{K_0 I_{pd}}{2\pi NC}}$$
(20)

The standard normalized form of the second order system is given by:

$$H(s) = \frac{2\zeta \omega_n s + \omega_n^2}{s^2 + 2\zeta \omega_n s + \omega_n^2} \quad (21)$$

The two equations are in the same form, and by equating terms we obtain the following analysis equations:

$$\omega_n = \sqrt{\frac{K_0 I_{pd}}{2\pi NC}}$$
(22)

$$\zeta = \frac{K_0 I_{pd} R}{4\pi N \omega_n} \quad (23)$$

Again referring to Fig. 2, the common PLL "error transfer function" is defined as:

$$H_{e}(s) = \frac{\theta_{ref} - (\theta_{out} / N)}{\theta_{ref}}$$
(24)

Similar analysis shows that H_e(s) may also be represented in normalized form as:

$$H_{e}(s) = \frac{s^{2}}{s^{2} + 2\zeta \,\omega_{n}s + \omega_{n}^{2}} \quad (25)$$

 $H_e(s)$ is a high pass function, whereas the phase transfer function H(s) is low pass. It will turn out that many of the modulation and noise responses of PLLs can be conveniently expressed using these functions, a fact not highlighted in standard references.

From these analysis equations 22 and 23 we obtain the following design equations:

$$C = \frac{K_0 I_{pd}}{2\pi N \omega_n^2} \quad (26)$$
$$R = \frac{4\pi N \omega_n \zeta}{K_0 I_{pd}} \quad (27)$$

Equations 26 and 27 are used to determine R and C based upon chosen values for natural frequency and damping factor. In practice a second capacitor is normally added in parallel with the series RC of the ideal second order loop filter, converting the loop to third order and adding additional phase shift.

Basic PLL SPICE Model

The design equations for the basic 2nd order PLL model will get the design into the ballpark. However, there are almost always additional poles in the loop that add phase shift that must be taken into account. A simple SPICE model is the easiest way to attack analysis of these effects and to get time domain responses. **Fig. 3** shows such a model, where the sampling nature of the loop is still being neglected. The model is based on representing phase as voltage. The integrating action of VCOs as integrators from



input voltage to output phase is performed by current sources driving capacitors. To make this analogy mathematically correct, note that the output phase of a VCO is given by:

$$\theta_{out}(t) = \int_0^t \omega(t) dt = K_0 \int_0^t V_{in}(t) dt \qquad (28)$$

The voltage on a capacitor driven by a voltage controlled current source is:

$$V_{out}(t) = \frac{1}{C} \int_0^t i(t) dt = \frac{g_m}{C} \int_0^t V_{in}(t) dt \qquad (29)$$

If capacitance is 1 Farad, then by setting $g_m = K_0$, the VCO may be replaced with the current source driving a capacitor, with output voltage numerically equal to VCO phase. This has been done in Fig. 3 with two such integrators representing a VCXO reference and the VCO. The current pump uses the actual value the chip provides (260 uA in the case of the rfPIC12C509), and the divider is represented as the fraction used (1/32 in the case of the rfPIC12C509). Since the bandwidth of this type PLL typically exceeds 100 kHz, it can track crystal oscillator frequency variation up to the limit that the crystal can be modulated. In the rfPIC12C509 the crystal is modulated by varying the capacitance in series with the crystal. This effect is modeled in Fig. 3 by a voltage driven VCXO. If the crystal oscillator is pushed near the limit of its modulation bandwidth (about 10-15 kHz), then its response to modulation is complex, though basically lowpass and thus amenable to modeling using filtering preceding the VCXO block of Fig. 3. This will be covered in later publications and application notes. The crystal oscillator of the rfPIC12C509 can typically be modulated up through 20 kbps. Since loop filters are typically designed to support PLL operation for noise and lock time, and not for response to FSK modulation of the PLL, some modifications of typical design parameters are called for in setting up the PLL for FSK modulation. Generally a larger than normal (normal being about 0.7) damping factor is used. This provides more phase margin than the typical 45 degrees, where phase margin is defined as 360 degrees minus the total open loop phase at unity gain crossover. This transmitter also provides for ASK modulation via turning the PA on and off, in which case the standard choices for damping factor and phase margin apply.

percent	bercent of the peak when the reference is square wave FSK modulated.							
R	C1	C2	Freq	Ko	Loop	Phase	Trans	Comment
			(MHz)	(MHz/V)	BW	Margin	Over	
							shoot	
680	3900 pF	0	315	239	220 kHz	73	31%	2nd order for reference
								nat. freq = 112 KHz
								damping = 0.94
680	3900 pF	390 pF	315	239	190 kHz	55	46%	Set up for U.S.
680	3900 pF	680 pF	315	239	175 kHz	47	58%	
680	3900 pF	1000 pF	315	239	155 kHz	39	76%	Note increasing overshoot
680	3900 pF	390 pF	380	323	250 kHz	54	45%	with decreasing margin
680	3900 pF	390 pF	470	79	80 kHz	45	67%	
1000	3900 pF	0	434	198	260 kHz	77	22%	Set up for European
1000	3900 pF	390 pF	434	198	220 kHz	52	40%	Last narrow BW
7500	39 pF	0	315	239	2.5 MHz	59	26%	Wide BW, nat. freq. =
	_							1.13 MHz, damping =1.03
7500	39 pF	4.7 pF	315	239	2.1 MHz	37	46%	
10K	39 pF	0	434	198	2.85 MHz	57	20%	nat. freq. = 1 MHz,
								damping $= 1.25$
10K	39 pF	4.7 pF	434	198	2.15 MHz	31	48%	
10K	39 pF	4.7 pF	434	198	2.15 MHz	31	0%	Square wave modulation
1								filtered with 100 KHz
								pole

Table 2: Loop filter values and loop parameters. Transient overshoot is the magnitude of the overshoot as a

Generally for ASK use a damping factor of 0.7 (45 degrees of phase margin) is will provide the fastest settling time while providing acceptable transient response and minimum lock time (about $2/f_n$, where f_n is the natural frequency).

Using the SPICE model shown, a set of values for loop filters for the rfPIC12C509 are given in Table 2. Some quite interesting trends may be observed in this table. First, the significant difference between loop bandwidth as defined by the open loop gain unity crossover and the "natural frequency" as is observed in common PLL design is evident. The loop bandwidth is typically several times the natural frequency, and unlike natural frequency is not independent of damping factor. However, as damping factor approaches zero (as loop resistor R approaches zero) the loop bandwidth will approach the natural frequency. The damping resistor pushes loop bandwidth up because the charge pump current flowing through it induces a greater voltage as R increases, and thus greater loop gain. The additional capacitor C2, necessary to suppress synthesizer spurs offset from the carrier by the loop sample rate, pushes loop bandwidth and phase margin back down.

FSK Modulation

FSK modulation within a phase locked loop can be provided by several methods. The simplest workable method that can provide modulation down to DC is to modulate the reference, as is done with the rfPIC12C509. For this product FSK modulation is implemented by keying a capacitor in series with the crystal, so it is shaped only by the natural response of the crystal (to be covered in detail in Part 4). The wideband PLL then follows this modulation, which it easily done since it is so much wider than the data bandwidth the crystal will allow (20 kbps). However, the PLL will generate undesired overshoot on step modulation. The data in Table 1 shows that decreases in loop phase margin will increase the overshoot of the VCO frequency output. Overshoots up to 50% of peak FSK are common if steps are not taken to

control it. The primary step taken by the user of such a part is to maintain the greatest phase margin consistent with meeting spur requirements (see Part 2). This is assisted by the fact that the crystal response cannot actually make a sharp step. It is a complex low pass filter function that does not instantly transition. The last row in Table 2 shows the large difference in step response that occurs when the modulating signal is even lightly filtered, so long as that filtering is well below the loop bandwidth. In that row the FSK is occurring at 10 kbps, is filtered with a first order low pass with pole at 100 kHz, and the loop bandwidth is 2.15 MHz. The loop is so fast that it tracks the changing reference almost perfectly, and hence does not overshoot. The difference between having this mild filtering, which is built into the crystal and cannot be avoided, is the difference between severe overshoot of 48% of peak value, and overshoot of less than 1%.

Analytically it may be easily shown that the transfer function from reference frequency input to VCO frequency output is also given by the phase transfer function of eq. 21. If the frequency response of the crystal to a modulating input $V_m(s)$, then the transfer function from the Vm(s) to the VCO output frequency is given by:

$$\omega_{out}(s) = V_m(s)X(s)H(s) \qquad (30)$$

 $V_m(s)$ may be replaced with another signal type, such as the step function modulated capacitance used in the rfPIC12C509. The transfer function X(s) may be crudely modeled as a first order low pass, and as mentioned above doing so in simulation will greatly reduce the overshoot of the FSK so long as loop bandwidth exceeds crystal modulation bandwidth.

Oscillator Phase Noise Analysis

Phase noise control in VCOs is a subject that has been well covered in previous work, but there are some new twists with respect to short-range radios. Phase noise is a particular problem in short-range radio due to the problem of lack of standards specifiying what the phase noise should be, and due to the low power consumption and Q of integrated VCOs. Some of these VCOs do not use bandpass resonators, and are effectively relaxation oscillators with a bandwidth from DC to past the oscillation frequency. Their Q is effectively about 1.0, as opposed to the loaded Q of 10 to 50 that could be attained with an LC oscillator. Since phase noise is inversely proportional to Q^2 , the phase noise of these oscillators is particularly poor. This problem is typically dealt with by use of a wide bandwidth PLL, which suppresses close in phase noise to approach the multiplied phase noise of the crystal reference oscillator. This also suppresses phase noise induced by other sources, such as flicker and digital noise on the power supply of the VCO and PLL. However, how wide does the PLL loop bandwidth need to be? A procedure to answer this critical question will be provided.

The phase noise of oscillators may be intuitively defined as the noise attached to and spread around the carrier that is measured in the frequency domain. In this sense it is much like intended modulation and if bad enough interferes with desired modulation. It is generally measured on a per Hz of frequency basis at some offset from the carrier and expressed in decibels relative to the total carrier power. We begin examination of the most important phase noise issues of low power VCOs as follows. The induced "sideband to carrier" ratio, a peak voltage magnitude based ratio, is developed from small signal FM theory and is given by:

$$\frac{SidebandMag}{CarrierMag}(f) = \frac{V_p(f)K_0}{2f}$$
(31)

where $V_p(f)$ is the peak value of a sinusoidal baseband modulating voltage at frequency "f" on the steering input to the VCO and K₀ is the gain of the VCO in Hz/V. The induced sidebands occur on both sides of the carrier. This equation is typically used to predict discrete spurs like synthesizer sidebands (using Fourier series to get sinusoids), but it is also useful for broadband noise sources. To apply to such sources a small transformation is needed. Since $V_p(f)$ is a peak value and noise sources would typically be expressed in rms, we may write the sideband to carrier power ratio based on rms noise voltage $V_n(f)$ as:

$$\frac{SidebandPwr}{CarrierPwr}(f) = \left(\frac{V_n(f)K_0}{\sqrt{2}f}\right)^2 \qquad (32)$$

The sideband to carrier power ratio of eq. (32) is the contribution of tuning input noise to the general phase noise L(f) that will be defined shortly. Taking $10\log(L(f))$ will give the contribution to phase noise from this source in units of dBc/Hz. An example of the effect of eq. 32 is the phase noise effect of the flicker noise of an op amp that is used in a loop filter or buffer driving a VCO. This is a seldom mentioned unpleasant fact that is actually one of the primary reasons behind the modern prevalence of the current pump PLL. The current pump is off more than 99% of the time, greatly reducing its flicker noise and often leaving the dominant noise source in the VCO input as the resistor in the passive loop filter. The phase noise contribution from large resistors in series with the tune line, or the resistor in the loop filter, can also be calculated from eq. 32. Another place it comes in extremely handy is the induced phase noise from power supply and ground. Even when the power supply is linearly regulated and supposedly quiet, it has flicker noise that can dominate the phase noise profile. To calculate this noise, one uses eq. 32 where K₀ becomes K_{0p}, the frequency change per volt of power supply change. This term is usually only a decade or so down from K₀, and can easily dominate. Many a designer has done a good job on the standard phase noise control issues and then been unpleasantly surprised by a power noise dominated phase noise as much as several tens of dB worse than predicted.

The oscillator design itself is inherently phase noisy even when the tune and power lines are sufficiently quiet. A relatively accurate expression for oscillator phase noise (derived from forms given in Refs. 6 and 7) from factors within the oscillator is given in equation 33 below:

$$S_{\phi}(f) = \frac{\left(\frac{f_{o}}{2Q}\right)^{2} \frac{GFkT}{P_{0}} f_{c}}{f^{3}} + \frac{\left(\frac{f_{o}}{2Q}\right)^{2} \frac{GFkT}{P_{0}}}{f^{2}} + \frac{\frac{GFkT}{P_{0}} f_{c}}{f} + \frac{GFkT}{P_{0}}$$
(33)

Actually, S ϕ is the double sided spectral density of phase fluctuation in rad²/Hz, which shall be related to what is commonly referred to as phase noise momentarily. This equation is basically Leeson's phase noise model with a flicker noise corner added, and with power on the output side of the amplifier to more clearly show the effect of active device gain G. The terms in this expression are defined as follows: f₀ = oscillator carrier or operating frequency

f = the offset frequency from the carrier at which phase noise is measured in a 1 Hz bandwidth

 f_c = flicker noise corner frequency of the oscillator active device, the frequency where flicker noise (1/f

noise) on the output of the device is equal to the thermal floor multiplied by gain and noise factor O = loaded O of the resonator

G = oscillator active device gain in compression

F = oscillator active device noise factor (not in dB) in compression, typically higher than the uncompressed noise factor

kT = Boltzman's constant and absolute temperature

 P_0 = output power of oscillator active device

The somewhat non-intuitive term "spectral density of phase fluctuation" may be, using a small angle approximation, interpreted as the noise spectral density ratio relative to carrier power commonly



called "phase noise". Phase noise is sometimes given as $L(F_0) = 10\log(S\phi/2)$ in units of dBc/Hz. Because we will have occasion here to consider both linear and dB units, let us make the more clear definitions:

$$L(f) = \frac{S_{\phi}(f)}{2} \tag{34}$$

$$LdB(f) = 10\log\left(\frac{S_{\phi}(f)}{2}\right) \qquad (35)$$

The factor of 1/2 comes from the convention that phase noise as a power spectral density is real and observed on one side, while the phase fluctuation spectral density has double the power in that it represents the phase fluctuation in a 1 Hz bandwidth on both sides of the carrier.

A typical VCO free running phase noise shape is shown in **Fig. 4**, where it will be noted there are only three main regions despite the fact that eq. 33 has four terms. The 1/f term has been left out because in most cases the $1/f^2$ term dominates it. For bipolar transistors the flicker corner can be from below 100 Hz to several KHz. For CMOS the flicker corner is typically from several tens of KHz to one MHz or a little more. The $1/f^2$ rise in phase noise begins at the resonator half bandwidth, or $f_0/2Q$. For the typical Qs and center frequencies of RF oscillators this is well beyond the 1/f corner, so the term f_c/f never catches up. However, for low frequency high Q oscillators such as crystal oscillators, the 1/f term can be noticed, particularly for CMOS with its high flicker noise.

Eq. 33 may be extended to include the effects of the tuning and power supply noise by adding the appropriate forms of eq. 32 to 33. This is a requirement for the high gain VCOs typical of integrated short-range radios. Doing this and converting to phase noise in watts (noise) per watt (carrier) per Hz via eq. 34 yields eq. 36 below: (36)

$$L(f) = \frac{\left(\frac{f_o}{2Q}\right)^2 \frac{GFkT}{2P_0} f_c}{f^3} + \frac{\left(\frac{f_o}{2Q}\right)^2 \frac{GFkT}{2P_0} + \left(\frac{V_{n1}(f)K_0}{\sqrt{2}}\right)^2 + \left(\frac{V_{n2}(f)K_{0p}}{\sqrt{2}}\right)^2}{f^2} + \frac{\frac{GFkT}{2P_0} f_c}{f} + \frac{GFkT}{2P_0} f_c}{f} + \frac{GFkT}{2P_0} f_c} + \frac{GFkT}{2P_0} f_c}{f} + \frac{GFkT}{2P_0} f_c$$

In Equation (36) V_{n1} is rms spectral noise density on the tune line, V_{n2} is rms spectral noise density on the power line, K_0 is VCO gain in Hz/V, and K_{0p} is the power supply pulling susceptibility of the VCO in Hz/V. This equation allows quick visualization of the design methods used to minimize oscillator phase noise noise. These are to maximize loaded Q, maximize output power (simultaneous voltage and current compression in the active device will extract the most power from the available budget), minimize flicker factor (bipolar is superior to FETs), minimize loop gain (3 to 6 dB over loop losses), minimize compressed noise figure (minimum compression helps here), minimize VCO gain and input noise, and minimize pulling frequency suceptibility and noise on the supply.

 V_{n1} is primarily resistive thermal noise and active device flicker noise. If an op amp drives a VCO input its flicker noise is likely to dominate the phase noise, especially for low power CMOS op amps. For current pump based PLLs the flicker noise will be low, since the pulse width of the current pumps will approach zero (unless the VCO is directly FSK modulated, when the phase detector will encode this modulation when the loop attempts to hold the VCO exactly on frequency). Thus, for current pump PLLs V_{n1} may be primarily thermal noise. Given the typically small current pump values, and typically wide loop bandwidth in short-range radios, this resistor is typically much larger than that used in the loop filter of a design such as a cell phone synthesizer. With the high VCO gain typical of short-range radios, its thermal noise is often quite noticeable. It is calculated using the standard equation:

$V_n(rms) = \sqrt{4kTR} \quad (37)$

The common practice of following a second order loop filter (2 capacitors, 1 resistor, which makes a 3rd order loop) with a second RC stage (resulting in a 4th order loop) must be viewed with caution in short-range radios. To avoid loading the loop filter with this last stage, this second resistor is normally made 5 to 10 times larger than the damping resistor and thus it has that much more thermal noise. Equations 36 and 37 in concert with the closed loop phase noise analysis described below should be used to check if this additional resistor and even the standard loop resistor are acceptable.

Closed Loop Synthesizer Phase Noise Analysis

The earlier statement that the wideband PLL could cover noise problems in the VCO will now be proved and analyzed. From eq. 32 it is clear that phase noise may be referred to input as a noise voltage in a way analogous to how the noise of amplifiers may be referred to input. If the oscillator is imagined as noiseless and all phase noise is induced by an imaginary rms noise voltage V_{nvo} (V Noise Vco Open loop) on the VCO tune input, and noting that total sideband to carrier power ratio is the same as L(f), then eq. 32 may be solved for V_{nvo} as:

$$V_{nvo} = \frac{f\sqrt{2L(f)}}{K_0}$$
(38)

This is the input referred open loop VCO noise, where L(f) is given by eq. 36. However, the open loop input referred noise will be modified by the closed loop action of the PLL. The PLL will reduce the noise within the loop bandwidth in the attempt to keep the phase error equal zero. It may be shown by basic analysis of Fig. 2 that the effect of the loop on the open loop input referred VCO phase noise is exactly equal to multiplying $H_e(s)$. That is, the injected noise V_{nvo} that models free running phase noise is modified by the loop to be the rms quantity V_{nvc} (Voltage Noise Vco Closed loop) residing directly on the tune voltage, and this voltage is:

$$V_{nvc} = V_{nvo} \left| H_e(s) \right| \tag{39}$$

This function can be used in the standard 2nd order normalized form given earlier, or for high accuracy in higher order loops it can be calculated based on the full set of intended and parasitic poles in the loop.

Next the question of crystal oscillator phase noise and its effect is addressed. Though the crystal oscillator is high Q and inherently low phase noise, its phase noise is much worse in CMOS high flicker processes, and is it then multiplied by divider value N through the PLL closed loop action. While the crystal reference for a cell phone is typically a well optimized bipolar device consuming about 2 mA, the crystal oscillator for a short range transmitter is typically 200 uA and often implemented with a CMOS digital gate active device that is typically higher noise figure and much higher flicker noise than a bipolar transistor. Referring to eq. 36, the increase in phase noise for this short range reference as compared to a cell phone reference would typically be on the order of 20-50 dB. This combination of factors is such that effect of the phase noise of the crystal oscillator on the total closed loop phase noise is definitely not negligible for short-range FSK systems. Analysis of the transfer functions of the closed loop PLL will show that

$$V_{nxc} = V_{nx} \frac{K_{ox}N}{MK_0} |H(s)| \quad (40)$$

In eq. 40 the following definitions apply:

 V_{nxc} = the closed loop rms noise that appears on the *VCO input* (not VCXO input) as a result of crystal oscillator phase noise

 V_{nx} = crystal oscillator noise referred to the crystal oscillator steering input (a VCXO)

 K_{ox} = crystal oscillator tune slope in Hz/V

M = value of any divider between the crystal oscillator and the phase detector

H(s) = the phase transfer function (these standard functions just keep coming up)

The method of representing crystal oscillator phase noise as referred to a tune input is useful because many references are VCXOs to allow exact frequency trim, which is then susceptible to noise on the tune line from thermal, flicker, and power supply noise sources that should be taken into account. The effect of supply noise on the crystal oscillator is taken into account just as it was for the VCO, though K_0 and K_{0p} for the crystal will be much lower than the corresponding tune slopes for the VCO. If the crystal oscillator is not a VCXO, then an arbitrary value for K_{0x} can be assumed for the purpose of this calculation.

The total noise V_{ntc} from the VCO and the crystal oscillator referred to the input of the VCO from these rms referred to VCO input voltages in the closed loop

state is:

$$V_{ntc} = \sqrt{V_{nvc}^2 + V_{nxc}^2} \qquad (41)$$

To get the total resulting closed loop phase noise, V_{ntc} is then applied back through eq. 32 to get:

$$Lc(f) = \left(\frac{V_{ntc}(f)K_0}{\sqrt{2}f}\right)^2 \tag{42}$$

The effect of the closed loop on PLL noise is especially dramatic for wideband loop, as shown in **Fig. 5**. Well inside the loop natural frequency the noise is suppressed 40 dB per decade (second order magnitude transfer function). If the loop natural frequency is out where the VCO phase noise is at 20 dB per decade and other noise sources do not limit loop action, then the phase noise will decline 20 dB per decade over that frequency segment. A common occurrence is for divider noise (not shown in this model) to limit this effect, typically so that the phase noise approximately flattens out at some offset well inside the loop bandwidth. Also, the loop can only



Figure 5: Typical wideband PLL VCO phase noise in the locked state. The integral of the area between the open and closed loop phase noise is the noise power removed by the loop.

reduce noise to the point of the multiplied crystal reference noise as given by eq. 40, which is why the phase noise turns around and starts rising again. However, crystal oscillators are very low phase noise due to their very high Q, and so despite degradations such as divider noise a wideband PLL can provide a high degree of phase noise clean up. It is this action that allows low Q integrated VCOs such as relaxation oscillators, usually running on unregulated supplies, to provide adequate performance for FSK modulation.

As an example, the model presented above is implemented in a MathCad model to analyze the performance of a typical BiCMOS transmitter implementation. The following basic parameters apply. **Crystal Oscillator:** Freq = 13.5625 MHz, loaded Q = 5000, flicker corner = 1 KHz, active device noise factor = 10, gain = 6 dB, current consumption = 250 uA, Zout = 2000 ohms, Pout = 63 uW. **VCO:** Freq = 434 MHz, Q = 1 relaxation oscillator, flicker corner = 1 KHz, active device noise factor = 10, compressed gain = 6 dB, current = 3 mA, Zout = 300 ohms, Pout = 1.35 mW, K₀ = 200 MHz/V. **PLL:** Natural freq.= 50 KHz, damping factor = 1.2, current pump = 260 uA, N = 32, M = 1, filter R = 470 ohms, filter C = 0.015 uF.

The resulting phase noise of the crystal oscillator, the open loop VCO, and the closed loop PLL are shown in **Figures 6, 7, and 8**. For the crystal oscillator with its very high Q the $1/f^3$ term is the first to rise above the floor. The VCO phase noise curve rising above 0 dB at very low offset frequency is not what actually happens, as physically LdB(f) must flatten at 0 dB. This error is due to the 1 Hz granularity assumed in the phase noise not being adequate as the offset approaches 1 Hz, which is particularly

apparent in this low Q high flicker noise case. The closed loop noise model shows the effect of the 50 KHz wide loop on the poor phase noise of the relaxation VCO. It may be noted that the phase noise at offsets lower than 1 KHz is equal to the crystal oscillator phase noise plus $10\log^2 B$, as would be expected from the PLL multiplying the reference by N (here N = 32). This phase noise will limit demodulated FSK signal to noise ratio to about 28 dB no matter how strong the receiver input signal to noise power ratio is.



FSK Communications Phase Noise Analysis Short-range radio systems are almost totally ASK or FSK modulation, since these modes are the lowest power and simplest to implement. For ASK systems phase noise is not a serious issue unless it is so bad that it places noticeable energy outside the receive bandwidth or fails regulatory requirements (Part 2). But for digital FSK (becoming especially popular in Europe) the phase noise sets an upper limit on the signal to noise ratio that may be achieved. It is desired for this limit to be high enough that in practice it is not a noticeable factor in bit error rate, which generally calls for the this limit to be 20 dB or more.

If a phase noisy unmodulated carrier is detected with a sensitive FM demodulator, the output will display a noise referred to as the residual frequency modulation, which is a noise that competes with the desired FSK. For integrated



Figure 7: Example VCO free running phase



Figure 8: Example short-range transmitter closed loop phase noise.

phase noise less than 1 rad², the square of rms residual FM due to phase noise over the bandwidth f_a to f_b is given by (Ref. 7):

$$\Delta f^{2} = 2 \int_{f_{a}}^{f_{b}} f^{2} L(f) df$$
(43)

This noise sets a limit on FSK signal to noise ratio (SNR) for intended FSK expressed as one sided rms frequency deviation f_{rms} that is given by:

$$\frac{S}{N}(phase \ noise \ bounded) = 10\log\frac{f_{rms}^2}{\Delta f^2} \ (44)$$

The limits of integration selected in (43) depend on the data rate and protocol used in the system, and the acceptable bit error rate (BER). The cascade of baseband filtering in the transmitter and receiver generally sets these limits. Sometimes this filtering may be pure low pass and extend all the way to DC, but it is common for something in the system or circuit design to force a low frequency high pass function such that the baseband filtering is actually bandpass. For example, FSK PLL modulation imposed by direct modulation of the VCO with correcting integrator to reduce distortion (see U.S. patent 6172579) cannot modulate all the way to DC. The rfPIC12C509 with FSK via the crystal reference does go all the way to DC, but the receiver may not necessarily go all the way to DC. For example, the receiver demodulator may be high pass filtered to remove DC offsets. Receiver automatic frequency control (AFC) also sets a lower limit on the frequency content of the demodulated FSK output, the effect of which is to place one or more high pass poles at the AFC system bandwidth. If any of these high pass poles are present, they suppress phase noise below the poles and provide a good number to use for f_a in eq. 43. However, if the protocol used has noticeable low frequency content, then AC coupling in the system above this content will degrade BER by removing desired energy. For example, at 20 kbps using a non-return to zero (NRZ) protocol an AC coupled high pass response will degrade BER the equivalent of only about 1/10 of a dB of SNR for a 10 Hz corner, but at 50 Hz will degrade BER by about 1 dB equivalent reduction in SNR. A Manchester format with zero DC content would have less susceptibility to high pass coupling in the system. A rule of thumb for selecting f_a for DC coupled systems is to set it a 0.1% for NRZ and 1% for Manchester, for which accuracy should be to within a small fraction of one dB. For the upper limit of integration f_b, select the lowest pole of the baseband low pass filtering, typically about half the data rate for binary FSK.

The phase noise limited FSK signal to noise ratio may now be examined, with highly enlightening results for the design of integrated short-range transmitters. Incorporating equations 43 and 44 into a MathCad model allows running up a variety of cases of process flicker noise, VCO Q, and PLL parameters. The final result of this is to give the necessary PLL bandwidth to provide a minimum acceptable SNR. The case examined is a data rate of 20 kbps, NRZ formatted, with a frequency deviation of 20 KHz peak to peak (modulation index = deviationPP/data rate = 1.0), with low pass filtering at 10 KHz (bandwidth-time product BT = 0.5). The limits of phase noise integration for this case are chosen as 10 Hz and 10 KHz. The phase noise cases will range from a BiCMOS process with flicker corner of 1 KHz to a CMOS process with flicker corner of 100 KHz, with VCO Qs ranging from 1 (relaxation oscillator) to 30 (LC with off die air core inductor), and with loop natural frequency ranging from 500 Hz to 100 KHz.

Flicker Corner (kHz)	Loop Nat. Freq. (kHz)	VCO Loaded O	Phase Noise Limited SNR (dB)	Comment
1	10	1	6.5	BiCMOS process, relaxation (no resonator) VCO
	20		14.9	
	30		20.7	Minimum acceptable
	50		28.5	
	100		37.7	
1	2	4	7.7	BiCMOS process, LC VCO with integrated inductor
	4		11.0	
	10		18.4	
	15		23	Need 12 kHz for 20 dB
	30		32	
1	1	10	13.1	BiCMOS process, LC VCO with heavily loaded external chip inductor
	4		18.3	
	10		25.6	Need 5.4 kHz for 20 dB
1	0.5	30	18.2	BiCMOS process, LC VCO with lightly loaded external air core inductor
	2		20.9	Need 1.5 kHz for 20 dB
	10		31.0	
100 KHz	50	1	17.7	CMOS process, relaxation (no resonator) VCO
	100		26.1	Need 64 kHz for 20 dB
100 KHz	20	4	12.7	CMOS process, LC VCO with integrated inductor
	50		23.1	Need 41 kHz for 20 dB
100 KHz	10	10	11.8	CMOS process, LC VCO with external chip inductor
	20		19.3	
	25		21.4	Need 23 kHz for 20 dB
100 KHz	10	30	18.5	CMOS process, LC VCO with external air core inductor
	20		23.3	Need 13.1 KHz for 20 dB

Table 3: Integrated PLL transmitter phase noise limited signal to noise ratio.

The results are shown in **Table 3**, from which a wealth of useful interpretations can be made. Interpolating the table for 20 dB SNR for the hypothetical BiCMOS process, relaxation oscillators need a loop natural frequency f_n of 30 kHz or more, integrated inductor LC VCOs need about 12 KHz or more, external chip inductor based LC VCOs need about 5.4 KHz or more, and external aircore based VCOs need f_n of about 1.5 KHz or more. For the hypothetical CMOS process shown, relaxation oscillators require f_n of about 64 kHz or more, on die inductors 41 kHz, chip inductors 23 kHz, and aircore inductors 13.1 kHz. In each of these cases the sample rate needs to be about 20 or more times the natural frequency, which sets the channel spacing that can be used for frequency agile designs using integer N synthesizers. Thus for BiCMOS transmitters we might expect integer N minimum channel steps of about 30 kHz minimum for external air core inductors up to about 600 kHz for no resonator relaxation

oscillators. For pure CMOS it would be expected for channel steps to range from a minimum of about 250 kHz for air core up to about 1.25 MHz for the relaxation VCO. These minimum channel step numbers could be reduced significantly for a fractional N synthesizer, but of course this takes more silicon and more design expertise. There are many approximations in this analysis, such as omission of divider noise, flicker noise on the supply (unknown), and crude estimates for flicker noise corners, but it does provide useful information on product planning that should be approximately correct.

Summary

Basic analysis highlighted a number of interesting points and limits in integrated short-range design. The equations for 2nd order current pump PLL design and the standard transfer functions not given in most references were provided. A simple SPICE model for simulation of higher order loops was developed. The standard PLL transfer functions H(s) and H_e(s) were shown to come up continuously in the modulation and noise behavior of the PLL based transmitter. Crystal based modulation such as that applied in the rfPIC12C509 can provide moderately well shaped (minimum overshoot) FSK when the loop bandwidth exceeds the low pass modulation bandwidth of the crystal reference. The standard form of Leeson's phase noise model was extended to induced phase noise to allow for the common degrading sources experienced in integrated PLL based transmitters based on high gain low Q VCOs and running on noisy supplies. A method and MathCad model of closed loop phase noise analysis was developed and used to predict necessary VCO Qs, power consumption, and PLL bandwidths to provide acceptable FSK signal to noise ratio under these harsh conditions. This model shows that even in the higher flicker noise CMOS processes it is possible to design integrated, narrowband, frequency agile, PLL based short-range radios that can provide acceptable phase noise within the limits of a lithium coin cell battery. As these types of radios develop, they can be expected to cost effectively compete with SAW based radios in the higher end of their market range. Even more interesting, and potentially more profitable, they may be expected to open up significant new applications where the "big system" functionality of tiny, low power, low cost, and highly intelligent short-range radios is required. Examples of these applications include two way control systems, wireless sensors, home automation and control, and other short-range data communications applications.

Next month, Part 4 will conclude this introductory short-range radio series with board level transmitter design issues and experimental results. In particular, crystal oscillator design, loop antenna design, and the practical issues of meeting regulatory requirements relevant to short-range radio will be covered.

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