Contents

1. Basic Specifications

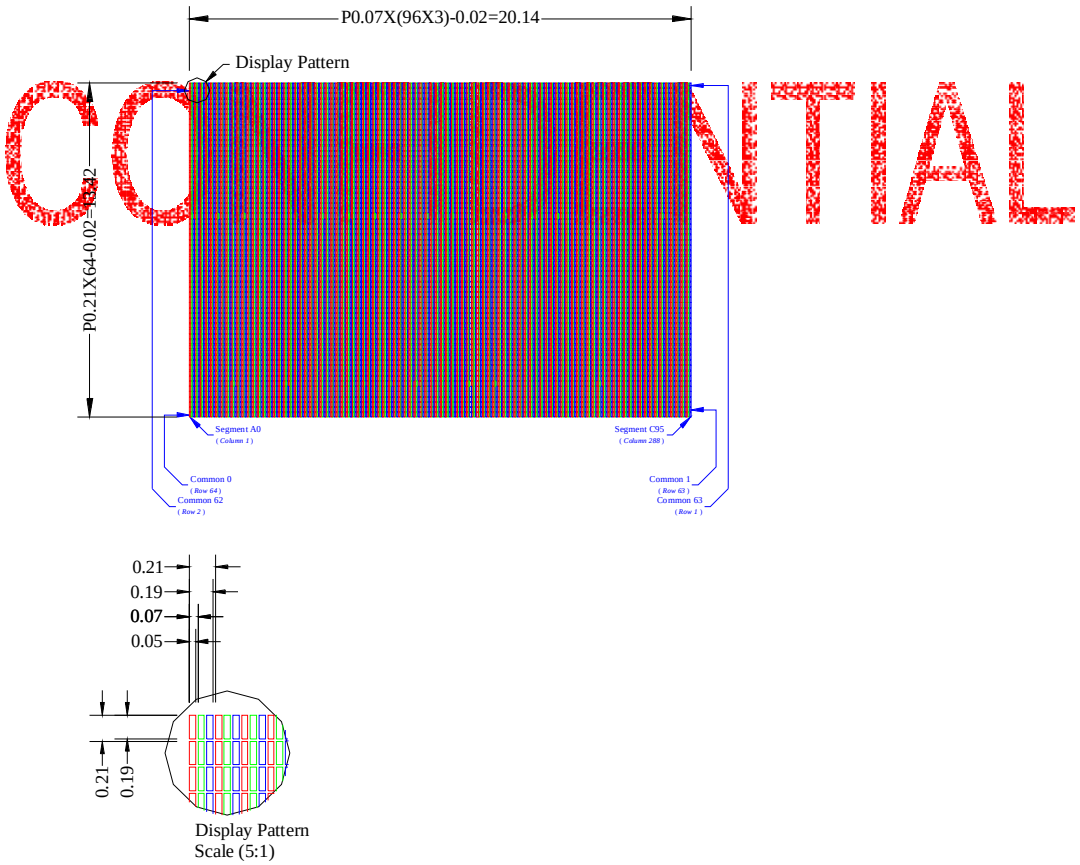
1.1 Display Specifications

1) Display Mode: Passive Matrix
2) Display Color: 65,536 Colors
3) Drive Duty: 1/64 Duty

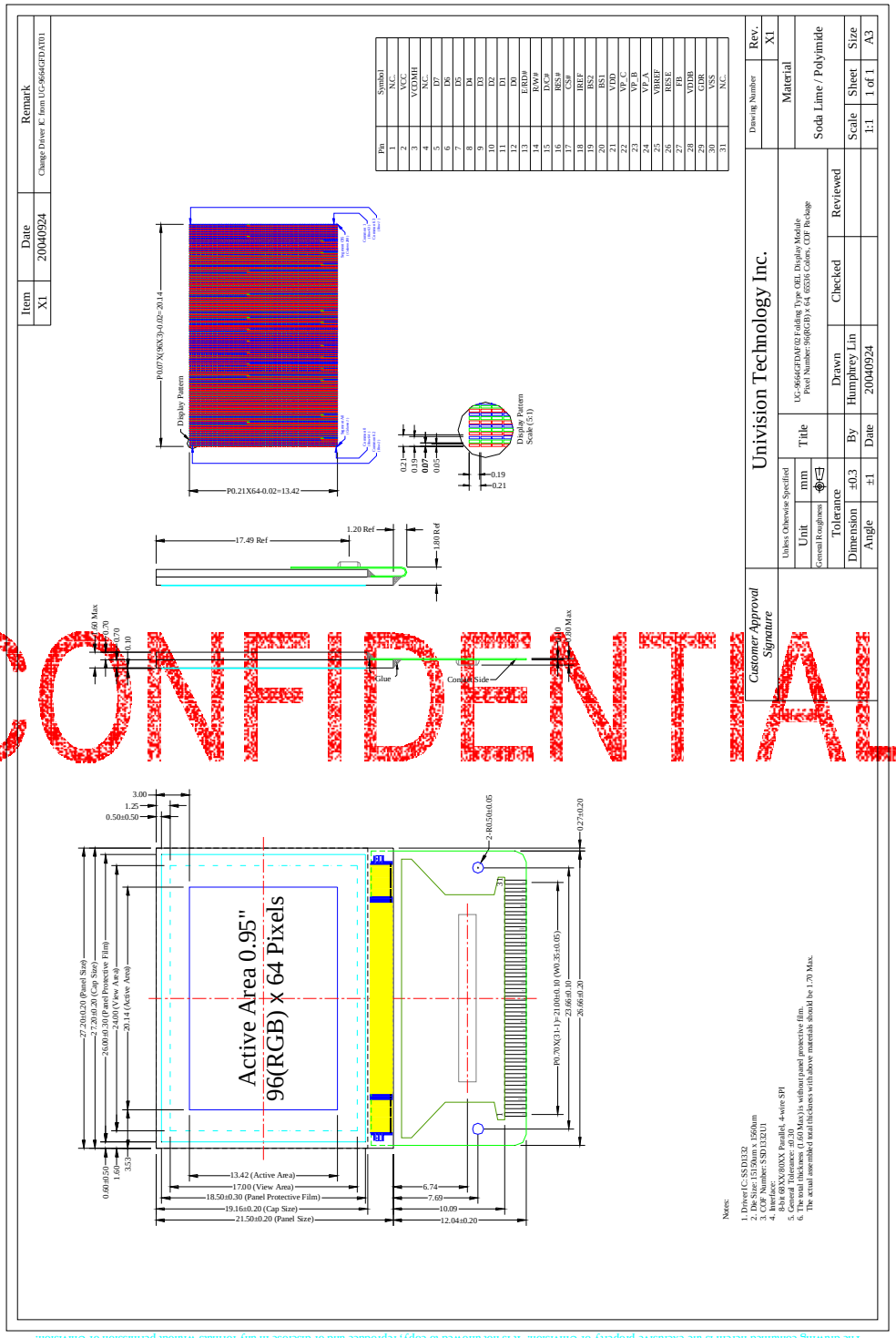
1.2 Mechanical Specifications

1) Outline Drawing: According to the annexed outline drawing number
2) Number of Pixels: 96(RGB) × 64
3) Panel Size: 27.20 × 21.50 × 1.60 (mm)
4) Active Area: 20.14 × 13.42 (mm)
5) Pixel Pitch: 0.07 × 0.21 (mm)
6) Pixel Size: 0.05 × 0.19 (mm)
7) Weight: 2.0 (g)

1.3 Active Area & Pixel Construction



1.4 Mechanical Drawing



1.5 Pin Definition

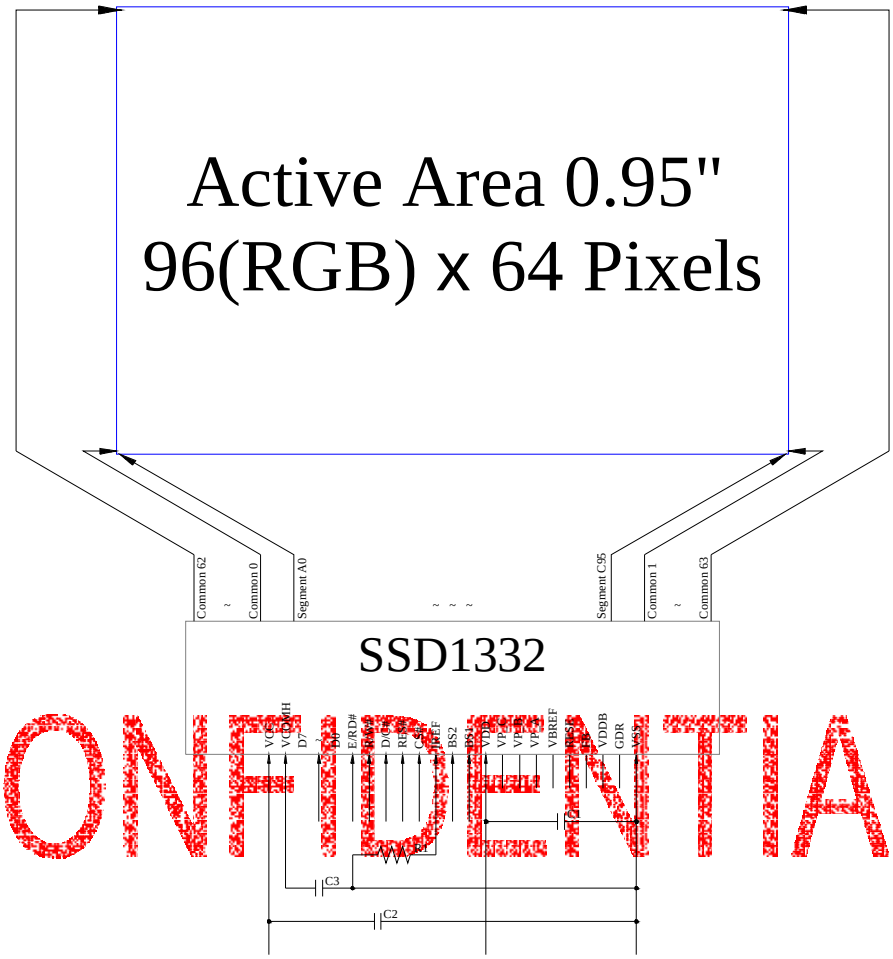
Pin Number	Symbol	I/O	Function
21	VDD	I	*Power Supply for Logic Circuit* This is a voltage supply pin. It must be connected to external source.
30	VSS	I	*Ground of OEL System* This is a ground pin. It also acts as a reference for the logic pins, the OEL driving voltages, and the analog circuits. It must be connected to external ground.
2	VCC	I/O	*Power Supply for OEL Panel* This is the most positive voltage supply pin of the chip. It can be supplied externally or generated internally by using internal DC/DC voltage converter.
24 23 22	VP_A VP_B VP_C	I	*External Voltage Reference for Pre-charge Signal* These pins are the pre-charge driving voltages for OEL driving segment pins SA0~SA95, SB0~SB95 and SC0~SC95 respectively. They can be supplied externally or internally generated by VP circuit. When internal VP is used, VP_A, VP_B, VP_C pins should be left open.
18	IREF	I	*Current Reference for Brightness Adjustment* This pin is segment current reference pin. A resistor should be connected between this pin and VSS. Set the current at 10uA.
3	VCOMH	I/O	*Voltage Output High Level for COM Signal* This pin is the input pin for the voltage output high level for COM signals. A capacitor should be connected between this pin and VSS.
28	VDDB	I	*Power Supply for DC/DC Converter Circuit* This is the power supply pin for the internal buffer of the DC/DC voltage converter. It must be connected to VDD when the converter is used. It must be floated when the converter is not used.
29	GDR	O	*Output for Connected External NMOS* This output pin drives the gate of the external NMOS of the booster circuit.
26	RESE	I	*Input for Connected External NMOS* This pin connects to the source current pin of the external NMOS of the booster circuit.
25	VBREF	I/O	*Voltage Reference for DC/DC Converter Circuit* This pin is the internal voltage reference of booster circuit. A stabilization capacitor, typ. 1uF, should be connected to VSS.
27	FB	I	*Feedback Input for DC/DC Converter Circuit* This pin is the feedback resistor input of the booster circuit. It is used to adjust the booster output voltage level (VCC).
20 19	BS1 BS2	I	*Communicating Protocol Select* These pins are MCU interface selection input. See the following table:

	68XX-parallel	80XX-parallel	Serial
BS1	0	1	0
BS2	1	1	0

1.5 Pin Definition (Continued)

Pin Number	Symbol	I/O	Function
16	RES#	I	*Power Reset for Controller and Driver* This pin is reset signal input. When the pin is low, initialization of the chip is executed.
17	CS#	I	*Chip Select* This pin is the chip select input. The chip is enabled for MCU communication only when CS# is pulled low.
13	E/RD#	I	*Read/Write Enable or Read* This pin is MCU interface input. When interfacing to a 68XX-series microprocessor, this pin will be used as the Enable (E) signal. Read/write operation is initiated when this pin is pulled high and the CS# is pulled low. When connecting to an 80XX-microprocessor, this pin receives the Read (RD#) signal. Data read operation is initiated when this pin is pulled low and CS# is pulled low.
14	R/W#	I	*Read/Write Select or Write* This pin is MCU interface input. When interfacing to a 68XX-series microprocessor, this pin will be used as Read/Write (R/W#) selection input. Pull this pin to "High" for read mode and pull it to "Low" for write mode. When 80XX interface mode is selected, this pin will be the Write (WR#) input. Data write operation is initiated when this pin is pulled low and the CS# is pulled low.
15	D/C#	I	*Data/Command Control* This pin is Data/Command control pin. When the pin is pulled high, the input at D7~D0 is treated as display data. When the pin is pulled low, the input at D7~D0 will be transferred to the command register. For detail relationship to MCU interface signals, please refer to the Timing Characteristics Diagrams.
5~12	D7~D0	I/O	*Host Data Input/Output Bus* These pins are 8-bit bi-directional data bus to be connected to the microprocessor's data bus. When serial mode is selected, D1 will be the serial data input SDIN and D0 will be the serial clock input SCLK.
1, 31	N.C.	-	*Reserved Pin (Supporting Pin)* The supporting pins can reduce the influences from stresses on the function pins.
4	N.C.	-	*Reserved Pin* The N.C. pins between function pins are reserved for compatible and flexible design.

1.6 Block Diagram



MCU Interface Selection: BS1 and BS2
Pins connected to MCU interface: D7~D0, E/RD#, R/W#, D/C#, RES#, and CS#
* VP_A, VP_B, VP_C, VBREF, RESE, FB, VDDB, GDR, and VSSB should be left float.

C1, C3: 4.7μF
C2: 10μF
R1: 910kΩ, R1 = (Voltage at IREF - BGGND) / IREF

2. Absolute Maximum Ratings

2.1 Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit	Notes
Supply Voltage	V_{DD}	-0.3	4.0	V	1, 2
Driver Supply Voltage	V_{CC}	0	15	V	1, 2
Operating Temperature	T_{OP}	-20	70	°C	-
Storage Temperature	T_{STG}	-30	80	°C	-

Note 1: All the above voltages are on the basis of "GND = 0V".

Note 2: When this module is used beyond the above absolute maximum ratings, permanent breakage of the module may occur. Also, for normal operations, it is desirable to use this module under the conditions according to Section 3. "Electrical Characteristics". If this module is used beyond these conditions, malfunctioning of the module can occur and the reliability of the module may deteriorate.

2.2 Regarding the Gradation

Although this module possesses the gradation function, respective gradation levels will vary depending on the production conditions etc. Also, the temperature range where the gradation function can be guaranteed will be -10°C~60°C.

3. *Electrical Characteristics*

3.1 DC Characteristics

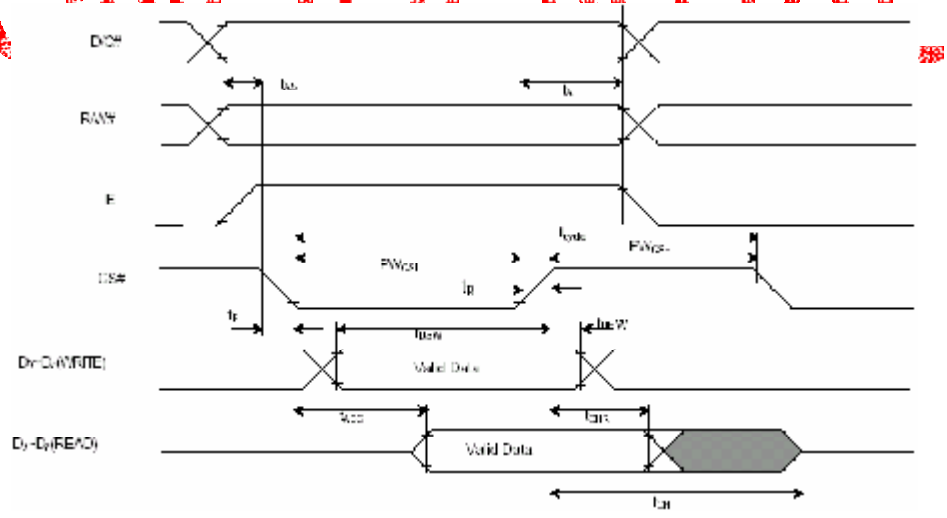
Characteristics	Symbol	Conditions	Min	Typ	Max	Unit
Supply Voltage	V_{DD}		2.5	2.8	3.5	V
Driver Supply Voltage	V_{CC}		-	11	-	V
High Level Input	V_{IH}	I_{out} = 100μA, 3.3MHz	0.8×V_{DD}	-	V_{DD}	V
Low Level Input	V_{IL}	I_{out} = 100μA, 3.3MHz	0	-	0.2×V_{DD}	V
High Level Output	V_{OH}	I_{out} = 100μA, 3.3MHz	0.9×V_{DD}	-	V_{DD}	V
Low Level Output	V_{OL}	I_{out} = 100μA, 3.3MHz	0	-	0.1×V_{DD}	V

3.2 AC Characteristics

3.2.1 68XX-Series MPU Parallel Interface Timing Characteristics:

Symbol	Description	Min	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	ns
t_{AS}	Address Setup Time	0	-	ns
t_{AH}	Address Hold Time	0	-	ns
t_{DSW}	Write Data Setup Time	40	-	ns
t_{DHW}	Write Data Hold Time	15	-	ns
t_{DHR}	Read Data Hold Time	20	-	ns
t_{OH}	Output Disable Time	-	70	ns
t_{ACC}	Access Time	-	140	ns
PW_{CSL}	Chip Select Low Pulse Width (Read) Chip Select Low Pulse Width (Write)	120 60	-	ns
PW_{CSH}	Chip Select High Pulse Width (Read) Chip Select High Pulse Width (Write)	60 60	-	ns
t_R	Rise Time	-	15	ns
t_F	Fall Time	-	15	ns

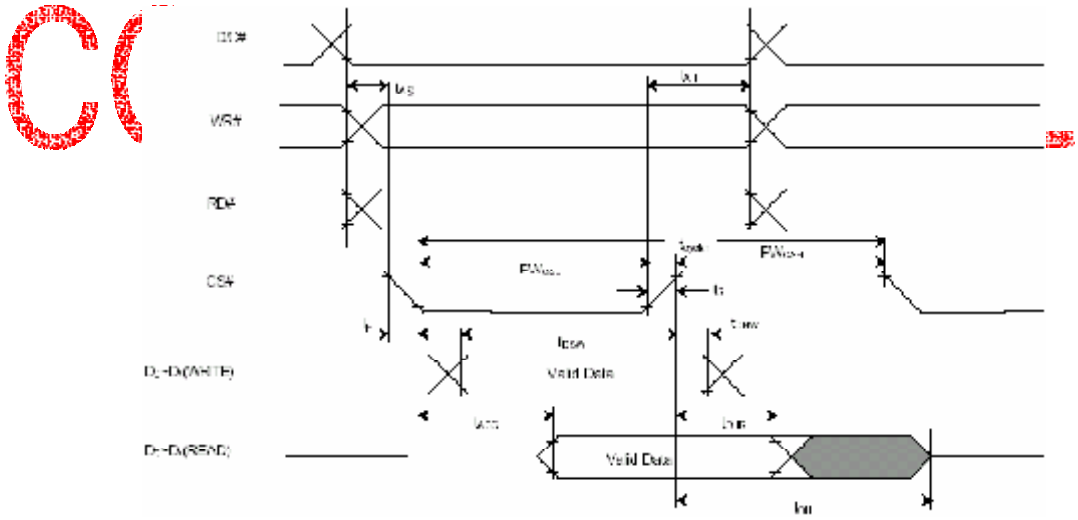
* All the timings should be based on 30% and 70% of V_{DD}-GND.



3.2.2 80XX-Series MPU Parallel Interface Timing Characteristics:

Symbol	Description	Min	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	ns
t_{AS}	Address Setup Time	0	-	ns
t_{AH}	Address Hold Time	0	-	ns
t_{DSW}	Write Data Setup Time	40	-	ns
t_{DHW}	Write Data Hold Time	15	-	ns
t_{DHR}	Read Data Hold Time	20	-	ns
t_{OH}	Output Disable Time	-	70	ns
t_{ACC}	Access Time	-	140	ns
PW_{CSL}	Chip Select Low Pulse Width (Read) Chip Select Low Pulse Width (Write)	120 60	-	ns
PW_{CSH}	Chip Select High Pulse Width (Read) Chip Select High Pulse Width (Write)	60 60	-	ns
t_R	Rise Time	-	15	ns
t_F	Fall Time	-	15	ns

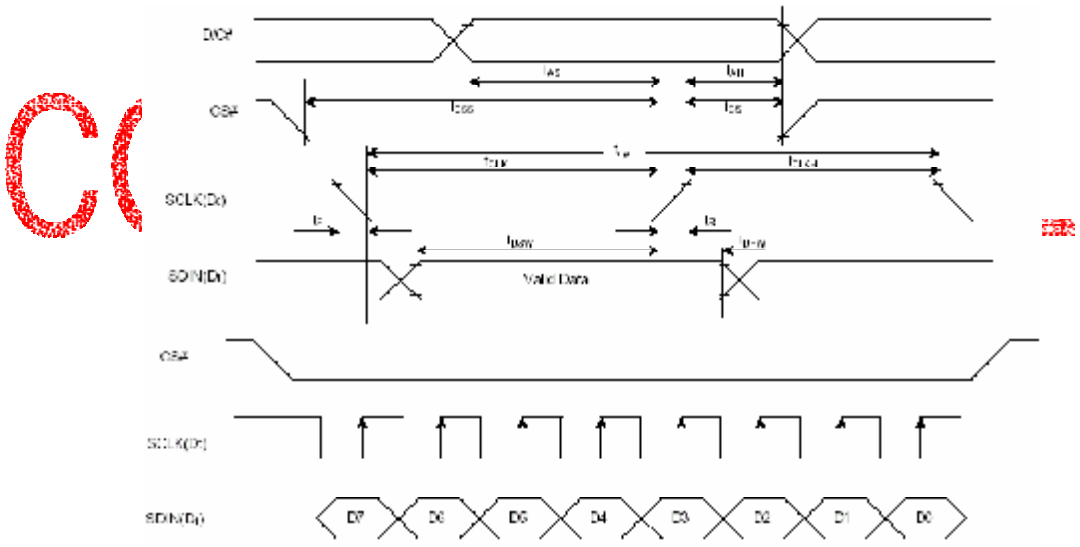
* All the timings should be based on 30% and 70% of V_{DD}-GND.



3.2.3 Serial Interface Timing Characteristics:

Symbol	Description	Min	Max	Unit
t_{cycle}	Clock Cycle Time	250	-	ns
t_{AS}	Address Setup Time	150	-	ns
t_{AH}	Address Hold Time	150	-	ns
t_{CSS}	Chip Select Setup Time	120	-	ns
t_{CSH}	Chip Select Hold Time	60	-	ns
t_{DSW}	Write Data Setup Time	100	-	ns
t_{DHW}	Write Data Hold Time	100	-	ns
t_{CLKL}	Clock Low Time	100	-	ns
t_{CLKH}	Clock High Time	100	-	ns
t_R	Rise Time	-	15	ns
t_F	Fall Time	-	15	ns

* All the timings should be based on 30% and 70% of V_{DD}-GND.



3.3 Optics & Electrical Characteristics

Characteristics	Symbol	Conditions	Min	Typ	Max	Unit
Brightness (White)	L_{br}	Display Average (Note 4)	70	90	-	cd/m^2
C.I.E. (White)	(x) (y)		-	0.40 0.44	-	
C.I.E. (Red)	(x) (y)		-	0.61 0.38	-	
C.I.E. (Green)	(x) (y)		-	0.38 0.57	-	
C.I.E. (Blue)	(x) (y)		-	0.12 0.19	-	
Dark Room Contrast	CR	Shown as below	-	>1:100	-	
View Angle			>160	-	-	degree

Note 3: Optical measurement taken at 1/64 duty, 100Hz Frame Rate, 0x0F Master Current Setting, 0xFF Individual Contrast Setting.

3.4 General Electrical Specification

Characteristics	Symbol	Conditions	Min	Typ	Max	Unit
Supply Voltage	V_{DD}		2.5	2.8	3.5	V
Driver Supply Voltage	V_{CC}	Note 4	10	11	12	V
Operating Current for V_{DD}	I_{DD}	Note 5	-	TBD	TBD	μA
		Note 6	-	TBD	TBD	μA
Operating Current for V_{CC}	I_{CC}	Note 5	-	TBD	TBD	mA
		Note 6	-	TBD	TBD	mA
Sleep Mode Current for V_{DD}	$I_{DD, SLEEP}$		-	TBD	-	μA
Sleep Mode Current for V_{CC}	$I_{CC, SLEEP}$		-	TBD	-	μA

Note 4: Brightness (L_{br}) and Driver Supply Voltage (V_{CC}) are subject to the change of the panel characteristics and the customer's request.

Note 5: V_{DD} = 2.8V, V_{CC} = 11V, Frame Rate = 100Hz, Master Current Setting = 0x0F, Individual Contrast Setting = 0xFF, 50% Display Area Turn on.

Note 6: V_{DD} = 2.8V, V_{CC} = 11V, Frame Rate = 100Hz, Master Current Setting = 0x0F, Individual Contrast Setting = 0xFF, 100% Display Area Turn on.

4. Functional Specification

4.1. Commands

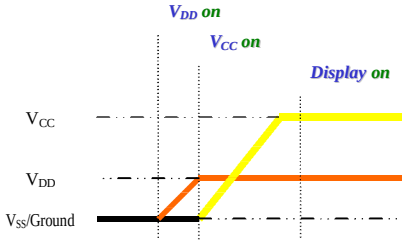
Refer to the Technical Manual for the SSD1332

4.2 Power down and Power up Sequence

To protect OEL panel and extend the panel life time, the driver IC power up/down routine should include a delay period between high voltage and low voltage power sources during turn on/off. Such that panel has enough time to charge up or discharge before/after operation.

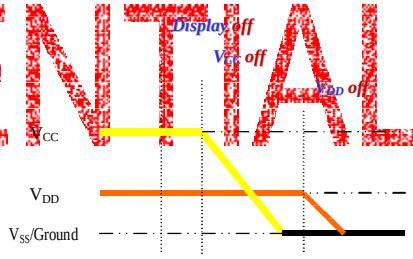
4.2.1 Power up Sequence:

1. Power up V_{DD}
2. Send Display off command
3. Clear Screen
4. Power up V_{CC}
5. Delay 100ms
   (when V_{DD} is stable)
6. Send Display on command



4.2.2 Power down Sequence:

1. Send Display off command
2. Power down V_{CC}
3. Delay 100ms
   (when V_{CC} is reach 0 and panel is completely discharges)
4. Power down V_{DD}



4.3 Reset Circuit

When RES# input is low, the chip is initialized with the following status:

1. Display is OFF
2. 64 MUX Display Mode
3. Normal segment and display data column and row address mapping (SEG0 mapped to column address 00H and COM0 mapped to row address 00H)
4. Shift register data clear in serial interface
5. Display start line is set at display RAM address 0
6. Column address counter is set at 0
7. Normal scan direction of the COM outputs
8. Master current control register is set at 0FH
9. Individual contrast control registers of color A, B, and C are set at 80H

4.4 Actual Application Example

Command usage and explanation of an actual example

<Initialization Setting>
Set Display Clock Divide Ratio / Oscillator Frequency
(10110011 with XXXXXXXX)

Set Display Offset
(10100010 with **XXXXXX)
* XXXXXX = 64 - Dummy Lines from Common 0
Set Multiplex Ratio
(10101000 with **XXXXXX)

Set Master Configuration
(10101101 with 10001XXX)
10001110 => 0x8E (External VCC Supply, Internal VCOMH Regulator & VP)

Set Display Start Line
(10100001 with **XXXXXX)
Set Segment Re-map & Data Format
(10100000 with XXXX**XX)
01100000 => 0x60

Set Master Current Control
(10000111 with ****XXXX)
Set Contrast Control for Color A
(10000001 with XXXXXXXX)
Set Contrast Control for Color B
(10000010 with XXXXXXXX)
Set Contrast Control for Color C
(10000011 with XXXXXXXX)

Set VPA, VPB, VPC Level for Color A, B, C
(10111XXX with XXXXXXXX)
Set VCOMH
(10111110 with *XXXXXXX)

Set Phase 1 & 2 Period Adjustment
(10110001 with XXXXXXXX)
Set Power Save
(10110000 with 000X00X0)

Set Display Mode (101001XX)
10100100 => 0xA4 (Normal)
Set Display On/Off (1010X111)
10101111 => 0xAF (Turns On)

<Display Boundary Setting>
Set Column Address
(00010101 with **XXXXXX for Start & **XXXXXX for End)

Set Row Address
(01110101 with ***XXXXX for Start & ***XXXXX for End)

If the noise is accidentally occurred at the displaying window during the operation, please reset the display in order to recover the display function.

5. *Reliability*

5.1 Contents of Reliability Tests

Item	Conditions	Criteria
High Temperature Operation	70℃, 120 hrs	The operational functions work.
Low Temperature Operation	-20℃, 120 hrs	
High Temperature Storage	80℃, 120 hrs	
Low Temperature Storage	-30℃, 120 hrs	
High Temperature/Humidity Operation	40℃, 90% RH, 48 hrs	
High Temperature/Humidity Storage	60℃, 90% RH, 120 hrs	
Thermal Shock	-30℃ ⇔ 80℃, 10 cycles 30 mins dwell	

* The samples used for the above tests do not include polarizer.
* No moisture condensation is observed during tests.

5.2 Lifetime

End of lifetime is specified as 50% of initial brightness.
An average operating lifetime of more than 5,000 hrs at room temperature is approached by 120 hrs @ 70℃ operating.

5.3 Failure Check Standard

After the completion of the described reliability test, the samples were left at room temperature for 2 hrs prior to conducting the failure teat at 23+5℃; 55−15% RH.

6. Outgoing Quality Control Specifications

6.1 Inspection Method:

6.1.1 Applicable Standard

MIL-STD-105E, Level II, Normal Inspection, Single Sampling

6.1.2 AQL

Partition	AQL	Definition
Major	0.65	Defects may lead to the failure of display function or the failure of passing the reliability criteria.
Minor	1.0	Defects do not affect all of the display functions, and have no impact to the reliability.

6.1.3 Inspection Condition

Test and measurement were conducted under the following conditions:

Temperature: 23 ± 5°C

Humidity: 55 ± 15 %RH

Distance between the Panel & Eyes of the Inspector: ≥ 30 cm

6.2 Inspection Criterion

Display Check in Active Area

Check Item	Classification	Criteria	
Non Operation/Display	Major	Not Allowable	
Flicker			
Missing Line or Pixel			
Wrong Display			
Cross Talk *			
Scratches, Fiber **	Minor	W ≤ 0.05 W ≤ 0.1, L ≤ 2 2 < L	Ignore n ≤ 3 n = 0
Dirt, Black Spot, White Spot, Greasy Dirt, Foreign Material, Dent, Bubbles **	Minor	Φ < 0.1 0.1 < Φ < 0.2 0.2 < Φ < 0.25 0.25 < Φ	Ignore n < 3 n < 1 n = 0
Fingerprint, Flow Mark	Minor	Not Allowable	

* In displays which manifests itself has the other shadowing, ghosting or streaking.

** Distance between any 2 defects should over 10mm.