RABBIT® 4000 MICROPROCESSOR

EASY REFERENCE

REGISTER LEGEND
Read/Write · Write Only · Read Only · Read (Special Behavior on Write Operation)
NOTE: ZERO MUST BE WRITTEN TO ALL UNUSED BITS

Processor Control

GLOBAL CLOCK MODULATOR REGISTERS
GCM0R (0x68) — 7 6 5 4 3 2 1 0
0 0 1 ns SPREADING; 0 1 0.25 ns SPREADING; 1 0 0.5 ns SPREADING; RESERVED MUST = 0
GCM1R (0x69) — 7 6 5 4 3 2 1 0
0 SPREADER OFF; 1 SPREADER ON; RESERVED MUST = 0

GLOBAL OUTPUT CONTROL REGISTER
GOCR (0x6E) — 7 6 5 4 3 2 1 0
CLK OUTPUT: 00 = CLK = PCLK; 01 = CLK = PCLK/2; 10 = CLK = LOW; 11 = CLK = HIGH
STATUS OUTPUT: 00 = LOW DURING FIRST OPCODE FETCH; 01 = LOW DURING INTERRUPT ACKNOWLEDGE; 10 = LOW; 11 = HIGH
/WDTOUT OUTPUT: 0 = LOW DURING WATCHDOG TIMEOUT (92.5 ms); 1 = LOW PULSE FOR DURATION OF 30.5 – 61 ms
/BUFEN OUTPUT: 00 = LOW FOR EXTERNAL I/O CYCLE; 01 = LOW FOR DATA MEMORY CYCLE; 10 = LOW; 11 = HIGH

GLOBAL POWER SAVE CONTROL REGISTER
GPSCR (0x0D) — 7 6 5 4 3 2 1 0
000 = SELF-TIMED CS DISABLE; 001 = 230 ns; 010 = 170 ns; 011 = 110 ns; 100 = 290 ns; 101 = 230 ns; 110 = 170 ns; 111 = 110 ns
SELF-TIMED CS READ ONLY
SELF-TIMED CS READ AND WRITE
0 = NORMAL CS FOR READS; 1 = SHORT CS TIMING FOR READS*
0 = NORMAL CS FOR WRITES; 1 = SHORT CS TIMING FOR WRITES*
000 = 32 kHz; 001 = RESERVED; 010 = 16.384 kHz; 101 = 8.192 kHz; 110 = 4.096 kHz; 111 = 2.048 kHz
CPU & PCLK
*AVOID IF AVAILABLE AT FULL SPEED!

GLOBAL CLOCK DOUBLE REGISTER
GCDR (0x0F) — 7 6 5 4 3 2 1 0
RESERVED MUST = 0
0 = DISABLE CLOCK DOUBLE; 1 = ENABLE CLOCK DOUBLE

00001	6 ns
00010	7 ns
00011	8 ns
00100	9 ns
00101	10 ns
00110	11 ns
00111	12 ns
01000	13 ns
01001	14 ns
01010	15 ns
01011	16 ns
01100	17 ns
01101	18 ns
01110	19 ns
01111	20 ns
10000	3 ns
10010	4 ns
10011	5 ns

TYPICAL DOUBLED CLOCK LOW TIME

GLOBAL CPU CONFIGURATION REGISTER
GCPU (0x2E) — 7 6 5 4 3 2 1 0
0 = FETCH PER SMODE; 1 = IGNORE SMODE
RD ONLY
SMODE
CPU VERSION (GCPU)

GLOBAL REVISION REGISTER
GREV (0x2F) — 7 6 5 4 3 2 1 0
REVISION (GREV)

PROCESSOR MODE SELECT

SMODE1	SMODE0	BOOTSTRAP OPERATION
0	0	BOOTSTRAP DISABLED, NORMAL PROCESSOR OPERATION (CODE FETCHED FROM MEMORY)
0	1	SLAVE PORT, SPDDR USED FOR BOOTSTRAP OPERATION
1	0	SYNCHRONOUS SERIAL: CLOCKED SERIAL PORT A ON PARALLEL PORT C USED FOR BOOTSTRAP OPER. MAX EXTERNAL CLOCK RATE = PCLK/6
1	1	ASYNCHRONOUS SERIAL: ASYNCH SERIAL PORT A ON PARALLEL PORT C USED FOR BOOTSTRAP OPER. REQUIRED BAUD RATE = 2400

REVISION IDENTIFIERS

	Marking	CPU	Revision
RABBIT 4000LCFP	ULLT	0x02	0x00
RABBIT 4000BGA	JCTT	0x02	0x00

Memory Management Unit

16 MEG; FFFFFF; E000; Y000; X000; 0000; 64K; XMEM; STACK SEGMENT; DATA SEGMENT; ROOT; 00000; 0E000; 0F000; 10000
SEGSIZE (0X13) R/W — 7 6 5 4 3 2 1 0
LOGICAL ADDRESS MAP; PHYSICAL ADDRESS MAP

EXTENDED PROGRAM COUNTER REGISTER — 15 … 8 7 6 5 4 3 2 1 0
12-BIT LOGICAL ADDRESS; 20-BIT PHYSICAL ADDRESS

STACK SEGMENT REGISTER (0x13) R/W — 7 6 5 4 3 2 1 0
STACKSEG; 16-BIT LOGICAL ADDRESS; 20-BIT PHYSICAL ADDRESS

STACKSEG H/L REGISTERS (0x18) (0x1A) — 15 … 8 7 6 5 4 3 2 1 0
16-BIT LOGICAL ADDRESS; 24-BIT PHYSICAL ADDRESS

DATA SEGMENT REGISTER (0x12) R/W — 7 6 5 4 3 2 1 0
DATASEG; 16-BIT LOGICAL ADDRESS; 20-BIT PHYSICAL ADDRESS

DATASEG H/L REGISTERS (0x1C) (0x1E) — 15 … 8 7 6 5 4 3 2 1 0
16-BIT LOGICAL ADDRESS; 24-BIT PHYSICAL ADDRESS

MEMORY BANK CONTROL REGISTERS
CONTROL REGISTER USED — ADDRESS

AI[19:18]		
00	MB0CR	(0x14) W
01	MB1CR	(0x15) W
10	MB2CR	(0x16) W
11	MB3CR	(0x17) W

MBxCR — 7 6 5 4 3 2 1 0
000 = 4 WS (5 FOR WRITES); 001 = 2 WS (3 FOR WRITES); 010 = 1 WS (2 FOR WRITES); 011 = 0 WS (1 FOR WRITES); 100 = PAS3; 101 = INVERT MSB; 110 = PAS3 LSB; 111 = INVERT LSB BANKSEL (AI=00:01:10:11)
0 = USE /OE0 & /WR0; 1 = USE /OE1 & /WE1
0 = USE /OE0 (READ ONLY); 1 = USE /OE1 (READ ONLY)
00 = USE /CS0; 01 = USE /CS1; 10 = USE /CS2

ADVANCED CHIP SELECT CONTROL REGISTERS
ACSR (0x410) — ACS1R (0x411)
000 = 7 WS 16-BIT / 1ST PAGE READ; 001 = 6 WS 16-BIT / 1ST PAGE READ; 010 = 5 WS 16-BIT / 1ST PAGE READ; 011 = 4 WS 16-BIT / 1ST PAGE READ; 100 = 3 WS 16-BIT / 1ST PAGE READ; 101 = 2 WS 16-BIT / 1ST PAGE READ; 110 = 1 WS 16-BIT / 1ST PAGE READ; 111 = 0 WS 16-BIT / 1ST PAGE READ
000 = 3 WS FOR LATER PAGE READS; 001 = 2 WS FOR LATER PAGE READS; 010 = 1 WS FOR LATER PAGE READS; 011 = 0 WS FOR LATER PAGE READS
000 = 9 (7 BASIC) WS FOR 16-BIT WRITE; 001 = 8 (6) WS FOR 16-BIT WRITE; 010 = 7 (5) WS FOR 16-BIT WRITE; 011 = 6 (4) WS FOR 16-BIT WRITE; 100 = 5 (3) WS FOR 16-BIT WRITE; 101 = 4 (2) WS FOR 16-BIT WRITE; 110 = 3 (1) WS FOR 16-BIT WRITE; 111 = ?

RAM SEGMENT REGISTER
RAMSR (0X448) — 7 6 5 4 3 2 1 0
COMPRIME VALUE FOR DATA MMU TRANSLATION WINDOW
00 = DISABLE RAM SEGMENT LIMIT CHECKING; 01 = SELECT DATA MMU TRANSLATION IF PC[15:12] = RAMSR[3:0]; 10 = SELECT DATA MMU TRANSLATION IF PC[15:11] = RAMSR[7:3]; 11 = SELECT DATA MMU TRANSLATION IF PC[15:12] = RAMSR[7:4]

MEMORY TIMING CONTROL REGISTER
MTCR (0x1F) W — 7 6 5 4 3 2 1 0
RESERVED MUST = 0; 0 = NORMAL TIMING FOR 1 = EXTENDED TIMING

MMU INSTRUCTION/DATA REGISTER
MMIDR (0x1D) R/W — 7 6 5 4 3 2 1 0
00 = USE 8-BIT INTERNAL I/O ADDRESSES; 01 = USE 13-BIT INTERNAL I/O ADDRESSES; 10 = RESERVED WRITE MUST = 0
0 = A16, MSB INVERSION INDEPENDENT OF INSTRUCTION/DATA; 1 = A16, MSB INVERSION FOR DATA ACCESS ONLY. (THIS ENABLES SEPARATE I AND D SPACE)
0 = NORMAL /CS1 OPERATION; 1 = FORCE /CS1 ALWAYS ACTIVE
0 = NORMAL; 1 = INVERT MSB ON DATASEG ACCESS
0 = NORMAL; 1 = INVERT A16 ON DATASEG ACCESS
0 = NORMAL; 1 = INVERT MSB ON ROOT ACCESS
0 = NORMAL; 1 = INVERT A16 ON ROOT ACCESS

MMU EXPANDED CODE REGISTER
MECR (0x18) — 7 6 5 4 3 2 1 0
000 = BANK SELECT ADDRESS IS A [19:18]; 001 = BANK SELECT ADDRESS IS A [20:19]; 010 = BANK SELECT ADDRESS IS A [21:20]; 011 = BANK SELECT ADDRESS IS A [22:21]; 100 = BANK SELECT ADDRESS IS A [23:22]; 111 = BANK SELECT ADDRESS IS A [18:17] OTHERS RESERVED
0000 = NORMAL; 100 = USE MBOCR FOR XPC ACCESS; 101 = USE MB1CR FOR XPC ACCESS; 110 = USE MB2CR FOR XPC ACCESS; 111 = USE MB3CR FOR XPC ACCESS OTHERS RESERVED

MEMORY ALTERNATE CONTROL REGISTER
MACR (0x0010) — 7 6 5 4 3 2 1 0
00 = DISABLE ALTERNATE FOR /CS1; 01 = ADVANCED 16-BIT OPERATION FOR /CS1 (NO BYTE WRITE); 10 = BASIC 16-BIT OPERATION FOR /CS1; 11 = ADVANCED 16-BIT OPERATION FOR /CS1 (BYTE WRITE)
0 = PAGE-MODE DISABLED FOR /CS1; 1 = PAGE-MODE ENABLED FOR /CS1
00 = 8-BIT OPERATION FOR /CS0; 01 = ADVANCED 16-BIT OPERATION FOR /CS0 (NO BYTE WRITE); 10 = BASIC 16-BIT OPERATION FOR /CS0; 11 = ADVANCED 16-BIT OPERATION FOR /CS0 (BYTE WRITE)
0 = PAGE-MODE DISABLED FOR /CS0; 1 = PAGE-MODE ENABLED FOR /CS0

Timer A

TIMER A CONTROL/STATUS REGISTER / TACSR (0xA0) — 7 6 5 4 3 2 1 0
TIMRA1 TIMRA0 TIMRA3 TIMRA2 TIMRA5 TIMRA4 TIMRA7 TIMRA6
(WRITE) 0 = CORRESPONDING TIMER A INTERRUPT IS DISABLED; 1 = CORRESPONDING TIMER A INTERRUPT IS ENABLED
(READ) 0 = CORRESPONDING TIMER A HAS NOT REACHED TERM. COUNT; 1 = CORRESPONDING TIMER A HAS REACHED TERM. COUNT
0 = MAIN CLOCK FOR TIMER A DISABLED; 1 = MAIN CLOCK FOR TIMER A ENABLED

TIMER A PRESCALE REGISTER / TAPR (0xA1) — 7 6 5 4 3 2 1 0
RESERVED MUST = 0; 0 = CLOCK = PCLK; 1 = CLOCK = PCLK/2
RESULTS IN ALL TIMER A TIMERS TO BE CLOCKED BY PCLK OR PCLK/2

TIMER A CONTROL REGISTER / TACR (0xA4) — 7 6 5 4 3 2 1 0
TIMRA3 TIMRA2 TIMRA1 TIMRA0 TIMRA3 TIMRA2 TIMRA1 TIMRA0
0 = CORRESPONDING TIMER A CLOCKED BY MAIN TIMER A CLK; 1 = CORRESPONDING TIMER A CLOCKED BY TIMER A1
00 = INTERRUPTS DISABLED; 01 = PRIORITY 1 INTERRUPT; 10 = PRIORITY 2 INTERRUPT; 11 = PRIORITY 3 INTERRUPT

TIME CONSTANT REGISTER
TAT1R (0xA3); TAT2R (0xA5); TAT3R (0xA7); TAT4R (0xA9); TAT5R (0xAB); TAT6R (0xAD); TAT7R (0xAF); TAT8R (0xA1); TAT9R (0xB3); TAT10R (0xA4)

PCLK or PCLK/2; TIMER A1; TIMER A2 … TIMER A7; TIMRA2 OUT; SERIAL E BAUD CLOCK; TIMRA3 OUT; SERIAL F BAUD CLOCK; TIMRA4 OUT; SERIAL G BAUD CLOCK; TIMRA5 OUT; SERIAL H BAUD CLOCK; TIMRA6 OUT; SERIAL A BAUD CLOCK; TIMRA7 OUT; SERIAL D BAUD CLOCK; INPUT CAPTURE; PWM; QUAD DECODER

Timer B

TIMER B CONTROL/STATUS REGISTER — 7 6 5 4 3 2 1 0
(WRITE) 0 = CORRESPONDING INTERRUPT IS DISABLED; 1 = CORRESPONDING INTERRUPT IS ENABLED
(READ) 0 = CORRESPONDING HAS NOT ENCOUNTERED A MATCH (STATUS BITS AND INTERRUPTS ARE CLEARED BY READ OF THIS REGISTER)
0 = MAIN CLOCK IS DISABLED; 1 = MAIN CLOCK IS ENABLED

TIMER B COUNTER REGISTER — 7 6 5 4 3 2 1 0
BITS [7:4] IGNORED
00 = CLOCKED BY PCLK/2; 01 = CLOCKED BY TIMER A1; 10 = CLOCKED BY PCLK/16; 11 = CLOCKED BY PCLK/256

TIMER B MATCH 1 REGISTER
(MSByte) BIT7 BIT6 BIT5 BIT4 BIT3 BIT2 BIT1 BIT0 — TBM1R (0xB2)
(LSByte) BIT7 BIT6 BIT5 BIT4 BIT3 BIT2 BIT1 BIT0 — TBL1R (0xB1)

TIMER B MATCH 2 REGISTER
(MSByte) BIT7 BIT6 BIT5 BIT4 BIT3 BIT2 BIT1 BIT0 — TBM2R (0xB4)
(LSByte) BIT7 BIT6 BIT5 BIT4 BIT3 BIT2 BIT1 BIT0 — TBL2R (0xB5)

TIMER B COUNT REGISTER
(MSByte) BIT15 BIT14 BIT13 BIT12 BIT11 BIT10 BIT9 BIT8 — TBCMR (0xB7)
(LSByte) BIT7 BIT6 BIT5 BIT4 BIT3 BIT2 BIT1 BIT0 — TBCLR (0xB7)

TIMER B 8 STEP LSB x REGISTER
TBSLR (0x00BA) TBSLZR (0x00BC)
LSB OF STEP SIZE FOR COMPARATOR

TIMER B 8 STEP MSB x REGISTER
TBSMR (0x00BB) TBSMZR (0x00BD)
MSB OF STEP SIZE FOR COMPARATOR

Timer C

TIMER C CONTROL/STATUS REGISTER
TCCSR (0x0500) — 7 6 5 4 3 2 1 0
0 = LIMIT NOT REACHED; 1 = LIMIT REACHED
0 = MAIN CLOCK IS DISABLED; 1 = MAIN CLOCK IS ENABLED

TIMER C CONTROL REGISTER
TCCR (0x0501) — 7 6 5 4 3 2 1 0
00 = CLOCKED BY PCLK/2; 01 = CLOCKED BY TIMER A1; 10 = CLOCKED BY PCLK/16; 11 = CLOCKED BY PCLK/256
00 = INTERRUPT DISABLED; 01 = PRIORITY 1 INTERRUPT; 10 = PRIORITY 2 INTERRUPT; 11 = PRIORITY 3 INTERRUPT

TIMER C COUNTER LOW REGISTER
TCNLR (0x0502) — 7 6 5 4 3 2 1 0
TIMER C COUNTER HIGH REGISTER
TCNHR (0x0590) — 7 6 5 4 3 2 1 0

TIMER C SET x LOW REGISTER
TCSSLR (0x0508); TCS1LR (0x050C); TCS2LR (0x0510); TCS3LR (0x0514) — 7 6 5 4 3 2 1 0
TIMER C SET x HIGH REGISTER
TCSSHR (0x0509); TCS1HR (0x050D); TCS2HR (0x0511); TCS3HR (0x0515) — 7 6 5 4 3 2 1 0

TIMER C RESET x LOW REGISTER
TCRSLR (0x050A); TCR1LR (0x050E); TCR2LR (0x0512); TCR3LR (0x0516) — 7 6 5 4 3 2 1 0
TIMER C RESET x HIGH REGISTER
TCRSHR (0x050B); TCR1HR (0x050F); TCR2HR (0x0513); TCR3HR (0x0517) — 7 6 5 4 3 2 1 0

TIMER C BLOCK ACCESS REGISTER
TCBAR (0x00F8) — 7 6 5 4 3 2 1 0
ACCESS REGISTER POINTED BY TCBPR

TIMER C BLOCK POINTER REGISTER
TCBPR (0x00F9) — 7 6 5 4 3 2 1 0
LSB OF REGISTER ADDRESS

External Interrupts

INTERRUPT 0 CONTROL REGISTER
I0CR (0x98) — 7 6 5 4 3 2 1 0
00 = DISABLE PD0 INTERRUPT; 01 = ENABLE PD0 FALLING EDGE; 10 = ENABLE PD0 RISING EDGE; 11 = ENABLE PD0 BOTH EDGE
00 = DISABLE PE4 INTERRUPT; 01 = ENABLE PE4 FALLING EDGE; 10 = ENABLE PE4 RISING EDGE; 11 = ENABLE PE4 BOTH EDGE
00 = DISABLE PE0 INTERRUPT; 01 = ENABLE PE0 FALLING EDGE; 10 = ENABLE PE0 RISING EDGE; 11 = ENABLE PE0 BOTH EDGE
00 = INTERRUPT DISABLED; 01 = INT0 PRIORITY 1; 10 = INT0 PRIORITY 2; 11 = INT0 PRIORITY 3

INTERRUPT 1 CONTROL REGISTER
I1CR (0x99) — 7 6 5 4 3 2 1 0
00 = DISABLE PD1 INTERRUPT; 01 = ENABLE PD1 FALLING EDGE; 10 = ENABLE PD1 RISING EDGE; 11 = ENABLE PD1 BOTH EDGE
00 = DISABLE PE5 INTERRUPT; 01 = ENABLE PE5 FALLING EDGE; 10 = ENABLE PE5 RISING EDGE; 11 = ENABLE PE5 BOTH EDGE
00 = DISABLE PE1 INTERRUPT; 01 = ENABLE PE1 FALLING EDGE; 10 = ENABLE PE1 RISING EDGE; 11 = ENABLE PE1 BOTH EDGE
00 = INT1 DISABLED; 01 = INT1 PRIORITY 1; 10 = INT1 PRIORITY 2; 11 = INT1 PRIORITY 3

EXTERNAL INTERRUPT HOLD TIME MUST BE AT LEAST 3 PERIPHERAL CLOCK CYCLES

Direct Memory Access

DMA MASTER CONTROL/STATUS REGISTER
DMCSR (0x0100) — 7 6 5 4 3 2 1 0
WR 0=NO EFFECT; WR 1=START/RESTART CHANNEL RD 0=CHANNEL DISABLED; RD 1=CHANNEL ENABLED

DMA MASTER CONTROL REGISTER
DMCR (0x0104) — 7 6 5 4 3 2 1 0
00 = DISABLE INTERRUPT; 01 = PRIORITY 1 INTERRUPT; 10 = PRIORITY 2 INTERRUPT; 11 = PRIORITY 3 INTERRUPT
00 = PRIORITY 0 TRANSFER; 01 = PRIORITY 1 TRANSFER; 10 = PRIORITY 2 TRANSFER; 11 = PRIORITY 3 TRANSFER

DMA MASTER TIMING CONTROL REGISTER
DMTCR (0x0105) — 7 6 5 4 3 2 1 0
000 = MIN 12 CLOCKS BETWEEN BURSTS; 001 = MIN 16 CLOCKS BETWEEN BURSTS; 010 = MIN 24 CLOCKS BETWEEN BURSTS; 011 = MIN 32 CLOCKS BETWEEN BURSTS; 100 = MIN 64 CLOCKS BETWEEN BURSTS; 101 = MIN 128 CLOCKS BETWEEN BURSTS; 110 = MIN 256 CLOCKS BETWEEN BURSTS; 111 = MIN 512 CLOCKS BETWEEN BURSTS

DMA x BUFFER COMPLETE REGISTER
D0BCR (0x0110); D1BCR (0x0112); D2BCR (0x0122); D3BCR (0x0132); D4BCR (0x0142); D5BCR (0x0152); D6BCR (0x0162); D7BCR (0x0172) — 7 6 5 4 3 2 1 0
0x = FIXED PRIORITY; 10 = ROTATE PRIORITY AFTER EVERY BYTE TRANSFER; 11 = ROTATE PRIORITY AFTER EVERY REQUEST IS SERVICED
000 = MAX 1 BYTE BURST; 001 = MAX 2 BYTE BURST; 010 = MAX 4 BYTE BURST; 011 = MAX 8 BYTE BURST; 100 = MAX 16 BYTE BURST; 101 = MAX 32 BYTE BURST; 110 = MAX 64 BYTE BURST; 111 = MAX 128 BYTE BURST
WR = LOAD COUNTER; RD = INCREMENTS BUFFER COUNTER

DMA x BUFFER UNUSED [7:0] REGISTER
D0BUR (0x0116); D1BUR (0x0118); D2BUR (0x0128); D3BUR (0x0138); D4BUR (0x0148); D5BUR (0x0158); D6BUR (0x0168); D7BUR (0x0178)

DMA x BUFFER UNUSED [15:8] REGISTER
D0BUHR (0x0117); D1BUHR (0x0119); D2BUHR (0x0129); D3BUHR (0x0139); D4BUHR (0x0149); D5BUHR (0x0159); D6BUHR (0x0169); D7BUHR (0x0179) — 15 … 8
STORES BITS OF BUFFER UNUSED LENGTH VALUE

DMA x TERMINATION BYTE REGISTER
D0TBR (0x010B); D1TBR (0x011B); D2TBR (0x012B); D3TBR (0x013B); D4TBR (0x014B); D5TBR (0x015B); D6TBR (0x016B); D7TBR (0x017B) — 7 6 5 4 3 2 1 0
MATCH VALUE

DMA x TERMINATION MASK REGISTER
D0TMR (0x0109); D1TMR (0x0119); D2TMR (0x0129); D3TMR (0x0139); D4TMR (0x0149); D5TMR (0x0159); D6TMR (0x0169); D7TMR (0x0179) — 7 6 5 4 3 2 1 0
TERMINATION BYTE MASK

DMA x STATE MACHINE REGISTER
D0SMR (0x0180); D1SMR (0x0190); D2SMR (0x01A0); D3SMR (0x01B0); D4SMR (0x01C0); D5SMR (0x01D0); D6SMR (0x0100); D7SMR (0x01F0) — 15 … 8 7 6 5 4 3 2 1 0
REFER TO MANUAL FOR DETAILS

DMA x STATUS REGISTER
D0SR (0x0181); D1SR (0x0191); D2SR (0x01A1); D3SR (0x01B1); D4SR (0x01C1); D5SR (0x01D1); D6SR (0x0101); D7SR (0x01F1) — 7 6 5 4 3 2 1 0
0 = NO EFFECT; 1 = AUTO-LOAD CHANNEL

DMA MASTER HALT REGISTER
DMHR (0x0102) — 7 6 5 4 3 2 1 0
0 = NO EFFECT; 1 = HALT CHANNEL

DMA x MASTER REQUEST 0 COUNTER REGISTER
DMR0CR (0x0106) — 7 6 5 4 3 2 1 0
000 = REQUESTS DISABLED; 001 = REQUEST ENABLED FROM PD2; 010 = REQUEST ENABLED FROM PE3; 011 = REQUEST ENABLED FROM PE7
000 = FALLING EDGE TRIGGERED (1 BYTE); 001 = RISING EDGE TRIGGERED (1 BYTE); 10 = ACTIVE LOW; 11 = ACTIVE HIGH
000 = REQUEST TO CHANNEL 0; 001 = REQUEST TO CHANNEL 1; 010 = REQUEST TO CHANNEL 2; 011 = REQUEST TO CHANNEL 3; 100 = REQUEST TO CHANNEL 4; 101 = REQUEST TO CHANNEL 5; 110 = REQUEST TO CHANNEL 6; 111 = REQUEST TO CHANNEL 7

DMA MASTER REQUEST 1 CONTROLREGISTER
DMR1CR (0X0107) — 7 6 5 4 3 2 1 0
000 = REQUESTS DISABLED; 001 = REQUEST ENABLED FROM PD3; 010 = REQUEST ENABLED FROM PE2; 011 = REQUEST ENABLED FROM PE6
000 = DISABLE INTERRUPT; 001 = ENABLE INTERRUPT; 10 = ACTIVE LOW; 11 = ACTIVE HIGH
000 = REQUEST TO CHANNEL 0; 001 = REQUEST TO CHANNEL 1; 010 = REQUEST TO CHANNEL 2; 011 = REQUEST TO CHANNEL 3; 100 = REQUEST TO CHANNEL 4; 101 = REQUEST TO CHANNEL 5; 110 = REQUEST TO CHANNEL 6; 111 = REQUEST TO CHANNEL 7

DMA AUTO-LOAD REGISTER
DMALR (0X0101) — 7 6 5 4 3 2 1 0
0 = NO EFFECT; 1 = AUTO-LOAD CHANNEL

DMA MASTER HALT REGISTER
DMHR (0x0102) — 7 6 5 4 3 2 1 0
0 = NO EFFECT; 1 = HALT CHANNEL

DMA TIMED REQUEST CONTROL REGISTER
DTRCR (0x0113) — 7 6 5 4 3 2 1 0
0 = TIMED REQUEST DISABLED; 1 = TIMED REQUEST ENABLED
00 = 1 BYTE PER REQUEST; 01 = RESERVED; 10 = TRANSFER UNTIL DISCRIPTOR IS COMPLETE; 11 = RESERVED
000 = REQUEST TO CHANNEL 0; 001 = REQUEST TO CHANNEL 1; 010 = REQUEST TO CHANNEL 2; 011 = REQUEST TO CHANNEL 3; 100 = REQUEST TO CHANNEL 4; 101 = REQUEST TO CHANNEL 5; 110 = REQUEST TO CHANNEL 6; 111 = REQUEST TO CHANNEL 7

DMA TIMED REQUEST DIVIDER HIGH REGISTER
DTRDHR (0x0117) — 15 … 8
MSB OF LIMIT VALUE FOR TIMER

DMA TIMED REQUEST DIVIDER LOW REGISTER
DTRDLR (0x0116) — 7 6 5 4 3 2 1 0
LSB OF LIMIT VALUE FOR TIMER

DMA DESCRIPTOR REGISTER
- CHANNEL 0 ADDRESSING SHOWN. ADD MULTIPLE OF 16 FOR CHANNELS 1 THRU 7 -

DOCR (0x0181) — 23 … 16 (0x181) → SEE BIT SETTINGS BELOW
DOLOR (0x0182) — 23 … 16 (0x182); 15 … 8 (0x183); 7 … 0 (0x184) — DMA LENGTH REG
DOAHR (0x0184) — 23 … 16 (0x186A); 15 … 8 (0x185); 7 … 0 (0x184) — DMA SOURCE ADDRESS
DOAAR (0x0188) — 23 … 16 (0x018A); 15 … 8 (0x0189); 7 … 0 (0x188) — DMA DEST ADDRESS
DOLAR (0x0180) — 23 … 16 (0x018E); 15 … 8 (0x018D); 7 … 0 (0x18C) — DMA LINK ADDRESS

DMA x CONTROL REGISTER
D0CR (0x0113); D1CR (0x0123); D2CR (0x0133); D3CR (0x0143); D4CR (0x0153); D5CR (0x0163); D6CR (0x0173); D7CR (0x0183) — 7 6 5 4 3 2 1 0
00 = CONTINUE TO NEXT DESCRIPTOR; 01 = FINAL DESCRIPTOR
0 = USE SEQUENTIAL ADDRESS; 1 = USE LINK ADDRESS FIELD
0 = NORMAL; 1 = SPECIAL LAST BYTE
0 = NO INTERRUPT ON COMPLETION; 1 = INTERRUPT ON COMPLETION
00 = SOURCE ADDRESS IS FIXED INTERNAL I/O ADDRESS; 01 = SOURCE ADDRESS IS FIXED EXTERNAL I/O ADDRESS; 10 = SOURCE ADDRESS IS MEMORY ADDR. AUTO-DECREMENT; 11 = SOURCE ADDRESS IS MEMORY ADDR. AUTO-INCREMENT
00 = DESTINATION ADDRESS IS FIXED INTERNAL I/O ADDR; 01 = DESTINATION ADDRESS IS FIXED EXTERNAL I/O ADDRESS; 10 = DESTINATION ADDRESS IS MEMORY ADDR. AUTO-DECREMENT; 11 = DESTINATION ADDRESS IS MEMORY ADDR. AUTO-INCREMENT

Serial Ports

SERIAL PORT x DATA REGISTER (SxDR)
SADR (0xC0); SBDR (0xD0); SCDR (0xE0); SDDR (0xF0) — 7 6 5 4 3 2 1 0
RD = RETURNS CONTENTS OF RCV BUFFER; WR = LOADS XMIT BUF WITH BYTE IN BYTE MODE

SERIAL PORT x ADDRESS REGISTER**
SAAR (0xC1); SBAR (0xD1); SCAR (0xE1); SDAR (0xF1) — 7 6 5 4 3 2 1 0
RD = RETURNS CONTENTS OF RCV BUFFER; W R = LOADS XMIT BUF WITH ADDRESS BYTE FOR TRANSMISSION (9TH BIT=1)

SERIAL PORT x LONG STOP REGISTER (SxLR)
SALR (0xC2); SBLR (0xD2); SCLR (0xE2); SDLR (0xF2) — 7 6 5 4 3 2 1 0
RD = RETURNS CONTENTS OF RCV BUFFER; WR = LOAD ADDRESS BYTE. MARK ADDRESS BIT = 1. HDLC MODE – WRITE LAST BYTE OF FRAME – ENABLE CLOSE FLAG TRANSMISSION

SERIAL PORT x STATUS REGISTER (SxSR)**
SASR (0xC3); SBSR (0xD3); SCSR (0xE3); SDSR (0xF3) — SESR (0xCB); SFSR (0xDB) — 7 6 5 4 3 2 1 0
RCV DATA REG FULL; RCV BUF ERROR; RCV BUF INT REQ; RCV PARITY ERROR; XMIT DATA REG EMPTY; XMIT ERROR; ALWAYS 0
0 = EMPTY; 1 = FULL, REQUESTS INTERRUPT. CLEARED WHEN RCV BUF READ
0 = BYTE IN RCV BUF IS DATA; 1 = BYTE IN RCV BUF IS ADDRESS
0 = RCV BUF NOT OVERRUN; 1 = RCV BUF OVERRUN. CLEARED WHEN RCV BUF READ
0 = BYTE IN RCV BUF HAS PARITY OK; 1 = BYTE IN RCV BUF HAS PARITY ERROR
0 = EMPTY. REQUESTS INTERRUPT 1 = FULL***
0 = IDLE REQUESTS INTERRUPT 1 = SENDING BYTE

SERIAL PORT x EXTENDED REGISTER
SAER (0xC5); SBER (0xD5); SCER (0xE5); SDER (0xF5); SEER (0xCD); SFER (0xDD)

ASYNC MODE (A,B,C,D,E,F) — 7 6 5 4 3 2 1 0
0000 = NRZ CODING; 0010 = NRZI CODING; 100 = BI-PHASE LEVEL CODING (MANCHESTER); 101 = BI-PHASE MARK CODING (FM1); 110 = BI-PHASE SPACE CODING (FM1); 111 = BI-PHASE MARK PARITY
0 = NORMAL CODING; 1 = R21 (3/16 kHZ)
0 = NORMAL BREAK; 1 = FAST BREAK
0 = ASYNC CLK = 16x; 1 = ASYNC CLK = 8x
0 = CHAR ASSY DURING BREAK; 1 = NO CHAR ASSY DURING BREAK

CLOCKED MODE (A,B,C,D) — 7 6 5 4 3 2 1 0
0 = NORMAL CLOCK; 1 = TIMED CLOCK
0 = TIMED BY TIMER B1; 1 = TIMED BY TIMER B2
0 = NORMAL CLK; INACTIVE HIGH, INT OR EXT CLK; 1 = INVERTED CLK; INACTIVE LOW, INT OR EXT CLK
0 = NORMAL CLK; INACTIVE LOW, INT OR EXT CLK; 1 = INVERTED CLK; INACTIVE HIGH, INT CLK
0 = NORMAL DATA BIT ORDER; 1 = REVERSE DATA BIT ORDER
0 = CLOCK INPUT FROM PARALLEL PORT D (SCER, SDER); 1 = CLOCK INPUT FROM PARALLEL PORT E (SCER, SDER)
TERMINATE NRZ; TERMINATE NRZI

HDLC MODE (E,F) — 7 6 5 4 3 2 1 0
000 = NRZ CODING; 010 = NRZI CODING; 100 = BI-PHASE LEVEL CODING (MANCHESTER); 101 = BI-PHASE MARK CODING (FM1); 110 = BI-PHASE SPACE CODING (FM1)
0 = NORMAL CODING; 1 = R21 (3/16 kHZ CODING)
0 = IDLE LINE COND. = FLAG; 1 = IDLE LINE COND. = ONE
0 = XMIT FLAG ON UNDERRUN; 1 = XMIT ABORT ON UNDERRUN
0 = SEPARATE EXTERNAL RCV/XMIT CLOCKS; 1 = COMBINED EXTERNAL RCV/XMIT CLOCKS (XMIT PIN)
TERMINATE NRZ; TERMINATE NRZI

SERIAL PORT x CONTROL REGISTER (SxCR)
SACR (0xC4); SBCR (0xD4); SCCR (0xE4); SDCR (0xF4) — 7 6 5 4 3 2 1 0
00 = NO OPERATION. IGNORED IN ASYNCH MODE; 01 = CLOCKED MODE: START BYTE R/V OPERATION; 10 = CLOCKED MODE: START BYTE A/V OPERATION; 11 = CLOCKED MODE: START BYTE A/V W/ INTERRUPT
00 = PARALLEL PORT C USED FOR INPUT; 01 = PARALLEL PORT D USED FOR INPUT; 10 = PARALLEL PORT E USED FOR INPUT; 11 = DISABLE RCV INPUT
00 = ASYNCH MODE: 8 BITS PER CHAR. 01 = ASYNCH MODE: 7 BITS PER CHAR. 10 = HDLC MODE: EXTERNAL CLOCK (INPUT) 11 = CLOCKED MODE: INTERNAL CLOCK (OUTPUT)
INTERRUPTS
00 = DISABLED; 01 = PRIORITY 1; 10 = PRIORITY 2; 11 = PRIORITY 3

SERIAL PORT x DIVISOR REGISTER
SADIVR (0xC7); SCDIVR (0xE7); SBDIVR (0xD7); SDDIVR (0xF7) — 7 6 5 4 3 2 1 0

SERIAL PORT x DIVIDER LOW REGISTER
SADLR (0xC6); SBDLR (0xD6); SCDLR (0xE6); SDDLR (0xF6) — 7 6 5 4 3 2 1 0

**ASYNCH ONLY (REFER TO MANUAL FOR CLOCKED SERIAL & HDLC) ***TX INTERRUPTS ARE CLEARED WITH A WRITE TO THE SxSR

Breakpoints

BREAKPOINT CONTROL REGISTER
BKCR (0x30B); BKCR (0x40B); B1CR (0x31B); B1ACR (0x41B); B2CR (0x32B); B2AR (0x42B); B3CR (0x33B); B3AR (0x43B); B4CR (0x34B); B4AR (0x44B); B5CR (0x35B); B5AR (0x45B); B6CR (0x36B); B6AR (0x46B); B7CR (0x37B); B7AR (0x47B) — 7 6 5 4 3 2 1 0
00 = NO BKPT ON EXECUTE MATCH; 01 = BKPT ON USER EXECUTE MATCH; 10 = BKPT ON SYSTEM EXECUTE MATCH; 11 = BKPT ON SYS OR USER EXECUTE MATCH
00 = NO BKPT ON READ MATCH; 01 = BKPT ON USER READ MATC