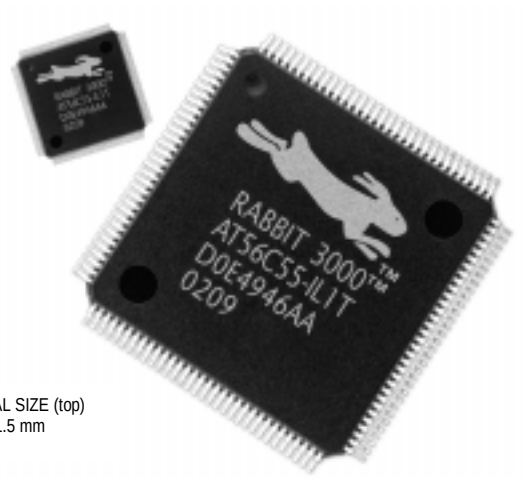
*Preliminary Summary*

# The New Rabbit 3000™ Microprocessor

## Key New Features

- **Low-EMI: typically <10 dB µV/m @ 3 m**
- **Ultra-low power modes**
- **1.5–3.6 V (5 V tolerant I/O)**
- **54 MHz clock speed**
- **56+ digital I/O**
- **6 serial ports supporting IrDA, SDLC/HDLC, Async, SPI**
- **Pulse capture and measurement**
- **Quadrature encoder inputs**
- **PWM outputs**




SHOWN ACTUAL SIZE (top)
16 x 16 x 1.5 mm

## Standard Features of Rabbit Processors

- **Glueless memory and I/O interface**
- **Direct support for 1 MB code/data space (up to 6 MB with glueless interface)**
- **Battery-backable real-time clock**
- **Watchdog timer**
- **Remote boot/program**
- **Slave port interface**

## Design Advantages

- **Extensive Ethernet/Internet support and royalty-free TCP/IP stack with source and sample programs**
- **Dynamic C® development environment for real-time development and debugging**
- **Blazingly fast performance for math, logic, and I/O**

### Why Rabbit?

Our fully supported embedded design systems include:

- Integrated development tools
- Free software libraries
- Free tech support
- Powerful core modules for rapid development

The new Rabbit 3000™ is an extremely low-EMI microprocessor designed specifically for embedded control, communications, and Ethernet connectivity. The Rabbit 3000 shares its instruction set and conceptual design with the proven Rabbit 2000™.

The Rabbit 3000 is fast—running at up to 54 MHz—and C-friendly, with compact code and direct software support for 1 MB of code/data space. Rabbit 3000 development tools include extensive support for Internet and network connectivity, with full source code for TCP/IP provided royalty free.

The Rabbit 3000 operates at 3.3 V (with 5 V tolerant I/O) and boasts 6 serial ports with IrDA, 56+ digital I/O, quadrature encoder inputs, PWM outputs, and pulse capture and measurement capabilities. It also features a battery-backable real-time clock, glueless interfacing, and ultra-low power modes. Its compact instruction set and high clock speeds give the Rabbit 3000 blazingly fast performance for math, logic, and I/O.

## Programming the Rabbit 3000

Microprocessor hardware and software development is easy for Rabbit users. The Rabbit 3000 is programmed using the industry-proven Dynamic C® Premier software development system from sister division Z·World.

Dynamic C is an integrated C compiler, editor, loader, and debugger created specifically for Rabbit-based systems. Developing software with Dynamic C is easy. Programming and debugging are accomplished by connecting a simple interface cable from a PC to a Rabbit-based target system or over Ethernet/Internet using appropriate accessory hardware.

Users can write, compile, and test C code, Assembly code, or even intermixed C and Assembly code without leaving the Dynamic C development environment. Debugging occurs while the application runs on the target, eliminating the need for costly in-circuit emulators. Alternatively, users can compile programs to an image file for later loading.

## Key Programming Features

- Fast compiler with one-step compiling and downloading to target
- Full-feature source and/or Assembly-level debugger
- Hundreds of functions in source-code libraries and sample programs
  - Exceptionally fast support for floating-point arithmetic and transcendental functions
  - RS-232 and RS-485 serial communications
  - Analog and digital I/O drivers
  - $I^2C$, SPI, GPS, Encryption, File System
- Powerful language extensions for cooperative or preemptive multi-tasking
- Loader utility program to load binary images into Z·World targets in the absence of Dynamic C
- Create your own source code libraries and augment on-line help by creating "function description" block comments using a special format for library functions
- Generate programs that use as much as 512K of data in SRAM and 512K of code in Flash or EPROM

## Royalty-Free TCP/IP

Full TCP/IP stack with source code is provided royalty free in Dynamic C. TCP/IP support includes PPP (with Dynamic C Premier), socket-level TCP and UDP, FTP, TFTP, HTTP (w/ SSI and CGI), DHCP client, SMTP mail client, PING, and POP3.

## The EMI-Free Microprocessor™

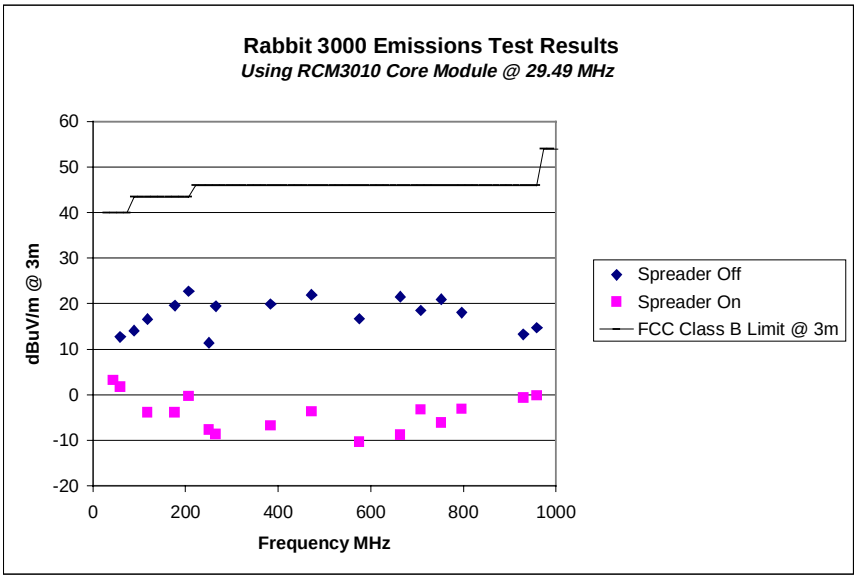
Government-mandated testing for electromagnetic interference (EMI) often proves a major headache for embedded systems design engineers. Unintentional electromagnetic radiation has the potential to derail development schedules with time-consuming board redesign or addition of costly EMI-reducing components.

The Rabbit 3000 has several powerful design features that practically eliminate EMI problems. These features are so effective that it is highly unlikely developers will ever experience EMI issues with the Rabbit 3000.

### *Low-EMI Features of the Rabbit 3000*

- A clock spectrum spreader reduces EMI amplitude derived from the clock by up to 25 dB.
- A clock doubler allows the external oscillator to operate at 1/2 the internal clock frequency.
- Separate power pins for the processor core and I/O ring prevent propagation of core noise to signal lines.
- Gated clocks in the internal logic blocks the clock-driving parts of the processor clock tree that are not in use for a particular instruction, reducing the amplitude of EMI generated by clock-related current surges.
- An auxiliary I/O bus limits loading and makes unnecessary the physical extension of fast data and address lines in the system.
- Bus architecture eliminates the need for routing the clock out of the processor.

The spectrum spreader is especially powerful, effectively reducing clock-related EMI and derivative signals by up to 25 dB—a design-critical amount, as devices often fail EMI tests by as little as 5 dB.



## Special Low-Power Features

The Rabbit 3000 contains a number of unique low-power features that make it highly suitable for battery-powered applications. The processor offers ultra-low-speed clock options that allow the chip to operate off of a divided (/2, /4, /8, /16) version of the 32.768 kHz clock or a divided (/2, /4, /6, /8) version of the fast clock.

Some types of Flash memory and SRAM consume power whenever the chip select is enabled, even if no signals are changing. The Rabbit 3000 has features to minimize the "chip select enabled" duty cycle to reduce this unnecessary power consumption when the Rabbit 3000 is running at divided clock speeds.

## Rabbit 3000 Development Kits

Our low-cost Rabbit 3000 Development Kits provide all the tools you need to develop Ethernet and non-Ethernet applications with the Rabbit 3000 microprocessor.

### *Rabbit 3000 Development Kits include:*

Microprocessor core module (with Rabbit 3000 processor, Flash, and SRAM), prototyping board, complete Dynamic C SE software development system (not a trial version) with TCP/IP software and documentation on CD-ROM, serial cable for programming and debugging, and AC adapter (U.S. kits only).

## Rabbit Instruction Set

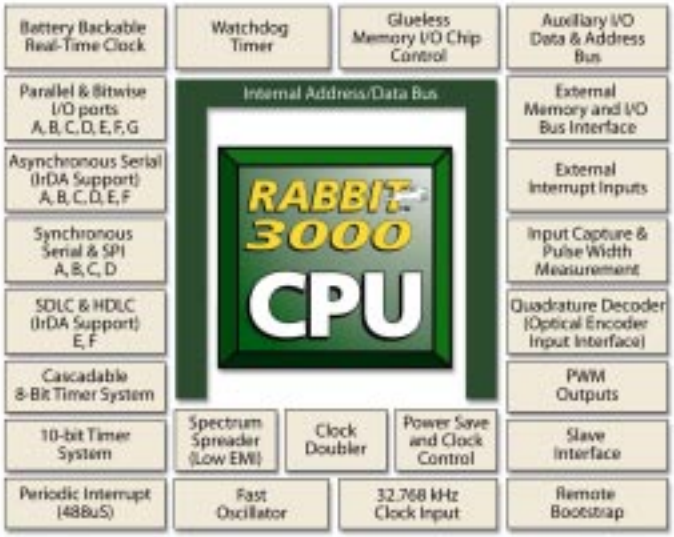
The Rabbit 3000 shares its instruction set and conceptual design with the proven Rabbit 2000 microprocessor. Rabbit processors feature an updated Z180-style architecture for higher performance. Several obsolete or redundant Z180 instructions have been dropped to allow efficient one-byte op-codes for new instructions. Existing Z180 Assembly language can be ported to the Rabbit with minimal changes.

Rabbit microprocessors have added important new instructions to improve the instruction set, especially from the standpoint of boosting the quality and execution speed of compiler-generated C code.

**Rabbit Instruction Set Improvements**

- Rabbit 3000 execution speed is up to 8 times faster than a Z80 or Z180.
- 16-bit loads and stores relative to the stack pointer and index registers greatly improve C code.
- New instructions make the alternate register set accessible and usable.
- I/O device access is now performed by prefixed memory instructions rather than dedicated I/O instructions.
- Long jumps and returns allow a full megabyte of code space.
- Long memory address stores and loads allow accessing a full megabyte of data.
- Instructions generally execute in 2 clocks per instruction byte, except for an additional clock required for some instructions to compute a memory address. The 16 x 16 multiply requires 12 clocks.

## Rabbit 3000 Block Diagram



## Peripherals

### Auxiliary I/O Bus

A common dilemma faced by many microprocessor system designers is resolving the conflict between the requirements of a fast memory bus that should have low address and data bus loading and an extensive I/O bus that shares the same lines and is heavily loaded.

With the Rabbit 3000, designers have the option of enabling completely separate buses for I/O and memory. The auxiliary I/O bus mirrors the processor's data bus on Port A and uses Port B to provide the processor's 6 least significant address lines for interface to external peripherals. The auxiliary bus is only active on I/O bus cycles.

Having a separate I/O bus reduces EMI and ground bounce by limiting the fast memory bus to a few close-in packages. Because the I/O bus is less active and slower than the memory bus, it can be extended farther without EMI and ground bounce problems.

### Parallel and Serial Ports

The Rabbit 3000 has 7 parallel ports, each with 8 bits, for a total of 56 I/O. Many of the ports share functionality with other devices, so depending on usage, some ports may be preempted by other functions such as serial I/O, the slave port, or the auxiliary I/O bus.

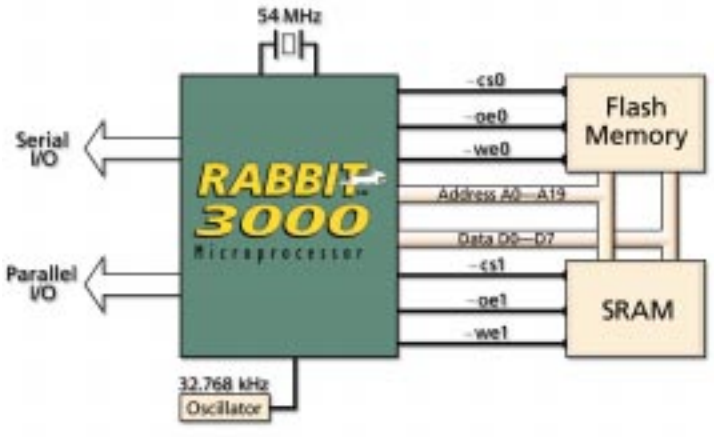
The Rabbit 3000 also offers 6 serial ports. All 6 are capable of communicating in asynchronous mode with baud rates up to 1/8 of the master clock. In addition, 4 ports support synchronous serial or SPI with baud rates of up to 1/4 of the processor clock if the internal serial clock is used and 1/6 the processor clock when an external serial clock is used. All ports support direct interface with standard serial communications transceivers.

The Rabbit 3000 provides 2 serial channels for SDLC/HDLC communications. SDLC/ HDLC allows full duplex synchronous serial communication with either an internal or external clock for communication. The following 5 types of signal modulation schemes are supported: NRZ, NRZI, biphase-level (Manchester), biphase mark (FM1), and biphase space (FM0).

The Rabbit 3000 also contains special hardware to support IrDA communications. All 6 asynchronous serial channels support SIR (serial infrared—115 Kbps), and the 2 SDLC/HDLC serial channels support MIR (medium infrared—up to 1.152 Mbps).

### Glueless Memory Interface

The Rabbit 3000 requires no external memory driver or interface logic. Its 20 address lines, 8 data lines, 3 chip select lines, 2 output enable lines, and 2 write enable lines can be interfaced directly to up to 6 memory devices (Flash or SRAM). Up to 1 MB of memory can be addressed directly, with the simplest possible hardware interface.




*Rabbit 3000* ***Basic Glueless Memory Interface***

## Integrated Slave Interface

The Rabbit 3000's built-in slave port makes it easy to use in a master-slave configuration. 3 data input, 3 data output, and 2 control registers simplify exchange of data between master and slave. 2 address lines and an 8-line data port, plus control signal lines, offer flexible interface possibilities whether the Rabbit 3000 is used as master, slave, or both.

## Remote Boot

The Rabbit 3000 can be remotely bootstrapped from serial port A in asynchronous, clocked serial (even using IrDA), or via the slave port interface. In Rabbit-based systems, the remote boot capability is used for configuring the Rabbit processor and for in-system programming of memory devices interfaced to the chip.

## Pulse Capture and Measurement

The Rabbit 3000 contains two Input Capture channels, each of which consists of a 16-bit counter clocked by the output of an internal timer. Each channel can be programmed to receive its inputs from one or two of 16 parallel port pins. The input capture channels can be used for a variety of functions, such as pulse width measurement or serial baud-rate detection.

## Quadrature Decoder

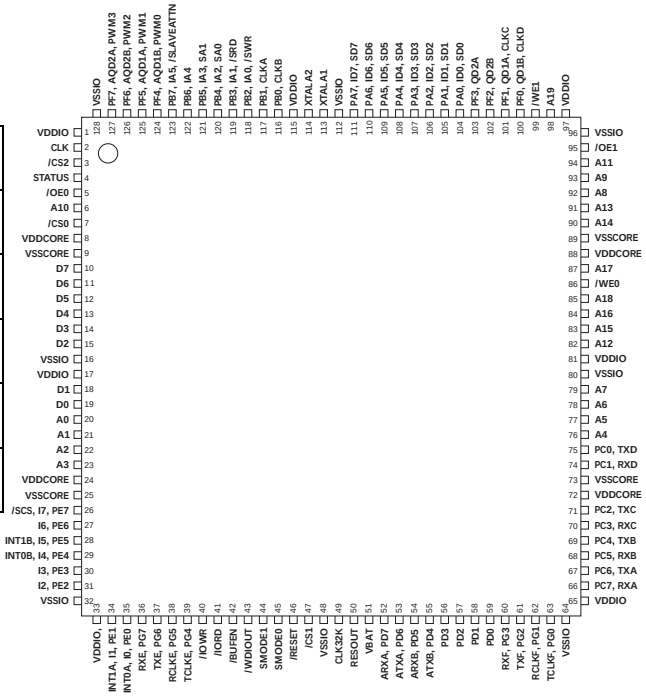
The Rabbit 3000 contains 2 quadrature decoder channels for direct interface to optical encoder units. Each quadrature decoder has 2 inputs, one serving as the normal input and the other as the quadrature input. An 8-bit up-down counter counts encoder steps in the forward and backward direction and requests interrupts when the count goes through the zero count in either direction.

## PWM Outputs

There are 4 independent PWM (pulse width modulation) output units in the Rabbit 3000. The PWM outputs generate a train of pulses periodic on a 1024 pulse frame with a duty cycle that varies from 0/1024 to 1024/1024. The units are driven by the output of an internal timer that can be programmed to vary the length of the pulses. The PWM outputs can be filtered and used to create a 10-bit D/A converter. They can also be used to directly drive devices that contain intrinsic filtering, such as motors or solenoids.

## Microprocessor Benchmark Comparisons

| Microprocessor | Dhrystone 1.1 (1,000s/sec) | Whetstone (1,000s/sec) | Sieve (milliseconds) |
|---|---|---|---|
| Rabbit 3000 @ 50 MHz Dynamic C | 6,570 | 813 | 53 |
| AMD 188ES @ 40 MHz Borland 3.31 C | 3,603 | 61 | 120 |
| Zilog ez80 @ 40 MHz Zilog C compiler | 2,914 | 20 | 158 |
| Dallas DS80C320 (8051) @ 33 MHz, Keil C | 1,251 | 140 | 160 |
| Phillips 80C51 @ 33 MHz Keil C | 598 | 61 | 350 |




**Rabbit 3000 Pinout**

# Rabbit 3000 Specifications and Performance

| Feature | Rabbit 3000 |
|---|---|
| Packaging | 128-pin LQFP* |
| Package Size | 16 × 16 × 1.5 mm |
| Operating Voltage | 1.5–3.6 V DC (5 V tolerant I/O) |
| Operating Current | 2 mA/MHz @ 3.3 V |
| Operating Temp. | –55°C to +85°C |
| Serial Ports | 6 |
| I/O Pins | 56 (plus multipurpose pins)<br>arranged in seven 8-bit ports |
| Memory Addressing Range | 20 lines (1 MB), more can be interfaced |
| Timers | Ten 8-bit and one 10-bit<br>with 2 match registers |
| Maximum clock speed | 54 MHz |
| Maximum crystal frequency main oscillator (may be doubled internally) | 27 MHz |
| 32.768 kHz oscillator | External |
| Maximum operating voltage | 3.6 V |
| Maximum I/O input voltage | 5.5 V |
| Spacing between package pins | 0.4 mm (16 mils) LQFP |
| Clock spectrum spreader (EMI reduction) | Yes |
| Clock modes | 1x, 2x, /2, /3, /4, /6, /8 |
| Power down modes | Sleepy (32 kHz)<br>Ultra-sleepy (16, 8, 2 kHz) |
| Low power memory control (chip select) | Short CS (CLK /4 /6 /8)<br>Self-timed (32, 16, 8, 2 kHz)<br>Current consumption,<br>sleepy mode: ~20 mA |
| Extended memory timing for high-frequency operation | Yes |
| Auxiliary I/O data/address bus | 8 data, 6 address lines |
| Serial ports capable of SPI/clocked serial | 4 (A, B, C, D) |
| Serial ports capable of SDLC/HDLC | 2 (E, F) |
| Async serial ports with support for IrDA communications | 6 |
| Serial ports with support for SDLC/HDLC | 2 |
| Maximum asynchronous baud rate | Clock speed/8 |
| Input pulse capture unit | 2 |
| Quadrature encoder inputs (quadrature decoders) | 2 |
| Dedicated PWM outputs | 4 |
| Glueless memory and I/O interface | 6 memory devices<br>8 I/O devices |
| Battery backable real-time clock | Yes |
| Watchdog timer/supervisor | Yes |
| Slave interface | Yes |
| Remote cold boot | Asynchronous IrDA<br>Asynchronous serial<br>Synchronous serial<br>Parallel (slave interface) |

* *TFBGA available in future (contact Rabbit Sales)*