Power Surveillance and Software Monitoring

Features

- Standby mode, maximum current 45 μA
- Reset output guaranteed for V_{DD} voltage down to 1.2 V
- Comparator for voltage monitoring, voltage reference 1.52 V
- Programmable reset voltage monitoring
- Programmable power-on reset (POR) delay
- Watchdog with programmable time window guarantees a minimum time and a maximum time between software clearing of the watchdog
- Time base accuracy ± 10%
- System enable ($\overline{EN}$) output offers added security
- TTL / CMOS compatible
- −40 to +85 °C temperature range
- On request extended temperature range, –40 to +125 °C
- DIP8 and SO8 packages

Description

The V6150 offers a high level of integration by voltage monitoring and software monitoring in an 8 lead package. A comparator monitors the voltage applied at the V_{IN} input comparing it with an internal 1.52 V reference. The power-on reset function is initialized after V_{IN} reaches 1.52 V and takes the reset output inactive after T_{POR} depending of external resistance. The reset output goes active low when the V_{IN} voltage is less than 1.52 V. The $\overline{RES}$ and $\overline{EN}$ outputs are guaranteed to be in a correct state for a supply voltage as low as 1.2 V. The watchdog function monitors software cycle time and execution. If the software clears the watchdog too quickly (incorrect cycle time) or too slowly (incorrect execution), it will cause the system to be reset. The system enable output prevents critical control functions being activated until software has successfully cleared the watchdog three times. Such a security could be used to prevent motor controls being energized on repeated resets of a faulty system.

Applications

- Automotive systems
- Cellular telephones
- Security systems
- Battery powered products
- Industrial electronics

Typical Operating Configuration

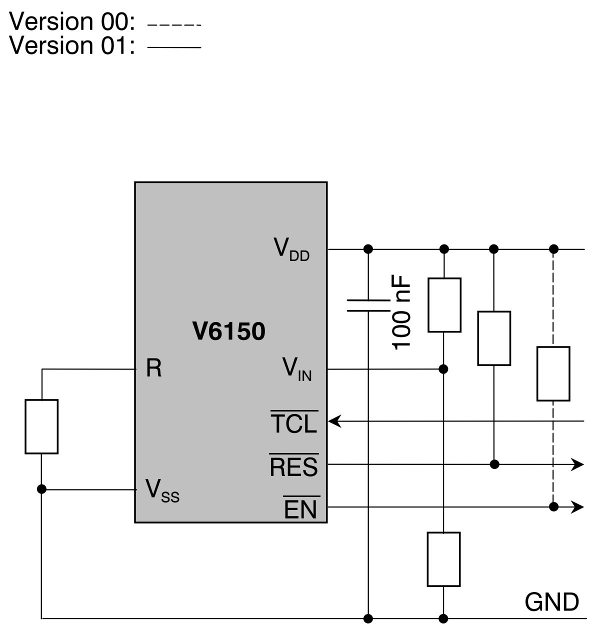


Fig. 1

Pin Assignment

DIP8 / SO8

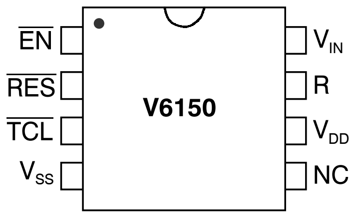


Fig. 2

Absolute Maximum Ratings

Parameter	Symbol	Conditions
Maximum voltage at V_{DD}	V_{DDmax}	V_{SS} + 7 V
Minimum voltage at V_{DD}	V_{DDmin}	V_{SS} − 0.3 V
Max. voltage at any signal pin	V_{MAX}	V_{DD} + 0.3 V
Min. voltage at any signal pin	V_{MIN}	V_{SS} − 0.3 V
Storage temperature	T_{STO}	-65 to +150 °C
Electrostatic discharge max. to MIL-STD-883C method 3015	V_{Smax}	1000 V
Max. soldering conditions	T_{Smax}	250 °C x 10 s

Table 1

Stresses above these listed maximum ratings may cause permanent damage to the device. Exposure beyond specified operating conditions may affect device reliability or cause malfunction.

Handling Procedures

This device has built-in protection against high static voltages or electric fields; however, anti-static precautions must be taken as for any other CMOS component. Unless otherwise specified, proper operation can only occur when all terminal voltages are kept within the supply voltage range. At any time, all inputs must be tied to a defined logic voltage level.

Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Units
Operating temperature[1)]	T_A	-40		+125	°C
Supply voltage[2)]	V_{DD}	1.2		5.5	V
$\overline{RES}$ & $\overline{EN}$ guaranteed[3)]	V_{DD}	1.2			V
Comparator input voltage	V_{IN}	0		V_{DD}	V
RC-oscillator programming	R	10		1000	kΩ

Table 2

1) The maximum operating temperature is confirmed by sampling at initial device qualification. In production, all devices are tested at +85 °C. On request devices tested at +125 °C can be supplied.

2) A 100 nF decoupling capacitor is required on the supply voltage V_{DD} for stability.

3) $\overline{RES}$ and $\overline{EN}$ ($\overline{EN}$ only for version 00) must be pulled up externally to V_{DD} even if they are unused. (Note: $\overline{RES}$ and $\overline{EN}$ are used as inputs by EM test.)

Electrical Characteristics

V_{DD} = 5 V ± 10%, C = 100 nF, T_A = -40 to +85 °C, unless otherwise specified

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Supply current in standby mode	I_{SS}	R_{EXT} = don't care, TCL = V_{DD}, V_{IN} = 0 V		23	45	µA
Supply current	I_{SS}	R_{EXT} = 100 kΩ, I/Ps at V_{DD}, O/Ps 1 MΩ to V_{DD}		75	120	µA
$\overline{RES}$ and $\overline{EN}$						
Output Low Voltage	V_{OL}	V_{DD} = 4.5 V, I_{OL} = 20 mA		0.4		V
	V_{OL}	V_{DD} = 4.5 V, I_{OL} = 8 mA		0.2	0.4	V
	V_{OL}	V_{DD} = 2.0 V, I_{OL} = 4 mA		0.2	0.4	V
	V_{OL}	V_{DD} = 1.2 V, I_{OL} = 0.5 mA		0.06	0.2	V
$\overline{EN}$						
Output High Voltage	V_{OH}	V_{DD} = 4.5 V, I_{OH} = −1 mA	3.5	4.1		V
	V_{OH}	V_{DD} = 2.0 V, I_{OH} = −100 µA	1.8	1.9		V
	V_{OH}	V_{DD} = 1.2 V, I_{OH} = −30 µA	1.0	1.1		V
$\overline{TCL}$ and V_{IN}						
$\overline{TCL}$ Input Low Level	V_{IL}	3V ≤ V_{DD} ≤ 5.5 V	V_{SS}		0.8	V
$\overline{TCL}$ Input High Level	V_{IH}	3V ≤ V_{DD} ≤ 5.5 V	2.0		V_{DD}	V
Leakage current $\overline{TCL}$ input	I_{LI}	V_{SS} ≤ V_{TCL} ≤ V_{DD}		0.05	1	µA
V_{IN} input resistance	R_{VIN}			100		MΩ
Comparator reference[1)]	V_{REF}	V_{DD} = 5 V, T_A = +25 °C	1.474	1.52	1.566	V
	V_{REF}	V_{DD} = 5 V	1.436		1.620	V
	V_{REF}	V_{DD} = 5 V, -40°C ≤ T_A ≤ +125°C	1.420		1.620	V
Comparator hysteresis[1)]	V_{HY}			2		mV

Table 3

1) The comparator reference is the power-down reset threshold. The power-on reset threshold equals the comparator reference voltage plus the comparator hysteresis (see Fig. 5).

I_{SS} Standby versus Temperature at V_{DD} = 5 V

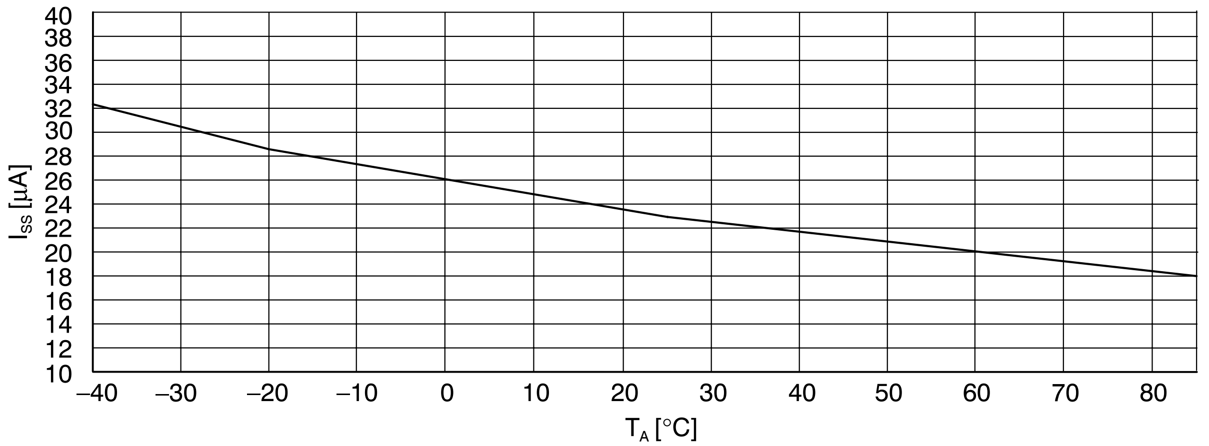


Fig. 3

Timing Characteristics

V_{DD} = 5.0 V ± 3%, C = 100 nF, T_A = –40 to +85 °C, unless otherwise specified

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Propagation delays:						
$\overline{TCL}$ to Output Pins	T_{DIDO}			250	500	ns
V_{IN} sensitivity	T_{SEN}		1	5	20	µs
Logic Transition Times on all Output Pins	T_{TR}	Load 10 kΩ, 50 pF		30	100	ns
Power-on Reset delay	T_{POR}	R_{EXT} = 123 kΩ, ±1%	90	100	110	ms
Watchdog Time	T_{WD}	R_{EXT} = 123 kΩ, ±1%	90	100	110	ms
Open Window Percentage	OWP			±0.2 T_{WD}		
Closed Window Time	T_{CW}			0.8 T_{WD}		
	T_{CW}	R_{EXT} = 123 kΩ, ±1%	72	80	88	ms
Open Window Time	T_{OW}			0.4 T_{WD}		
	T_{OW}	R_{EXT} = 123 kΩ, ±1%	36	40	44	ms
Watchdog Reset Pulse	T_{WDR}			T_{WD} / 40		
	T_{WDR}	R_{EXT} = 123 kΩ, ±1%		2.5		ms
T_{CL} Input Pulse Width	T_{TCL}		150			ns

Table 4

Timing Waveforms

Watchdog Timeout Period

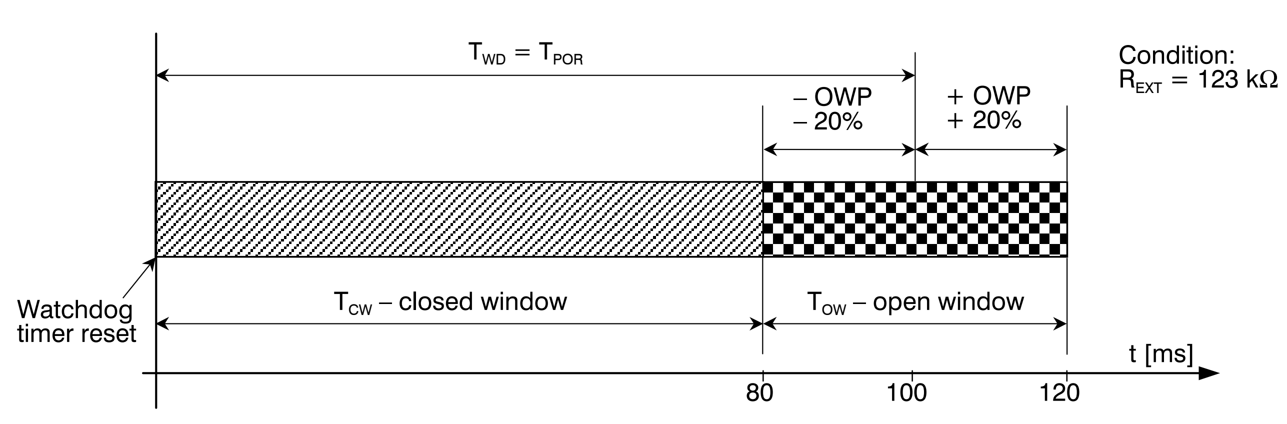


Fig. 4

Voltage Monitoring

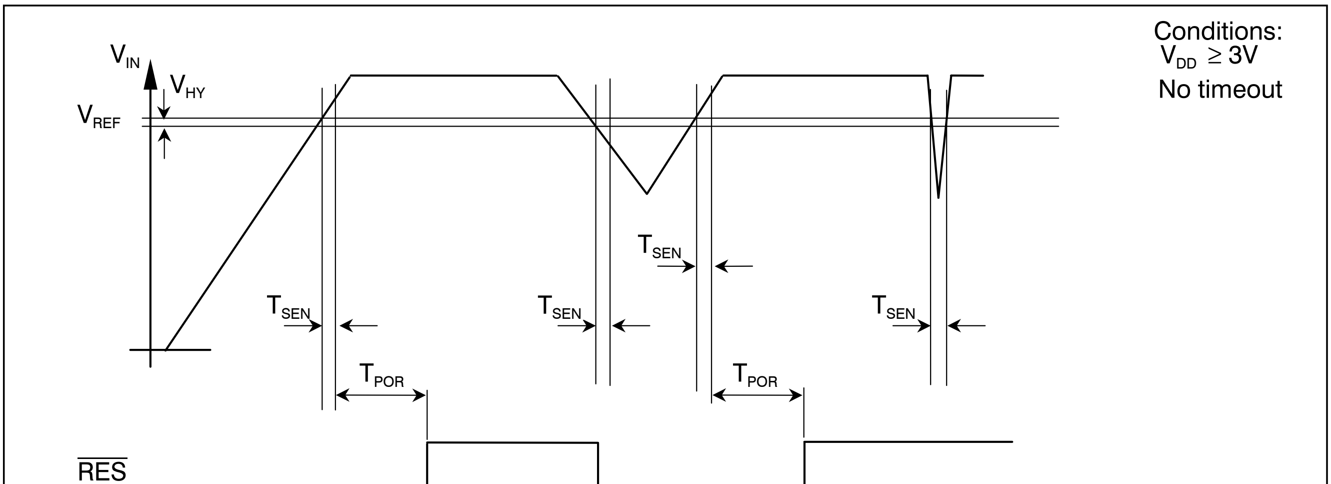


Fig. 5

Timer Reaction

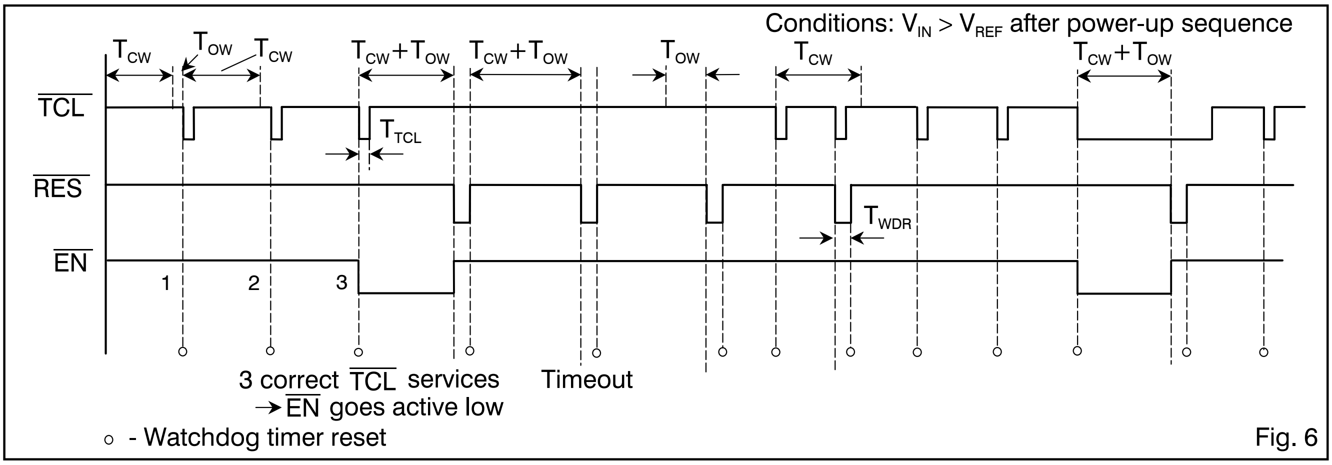


Fig. 6

Combined Voltage and Timer Reaction

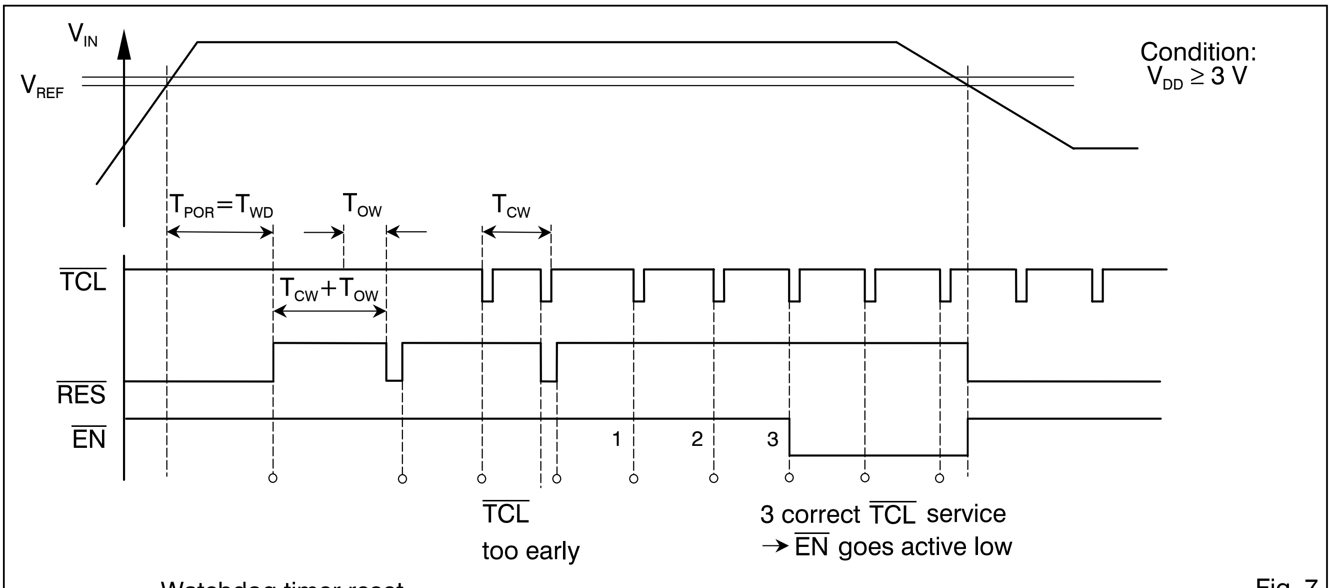


Fig. 7

Block Diagram

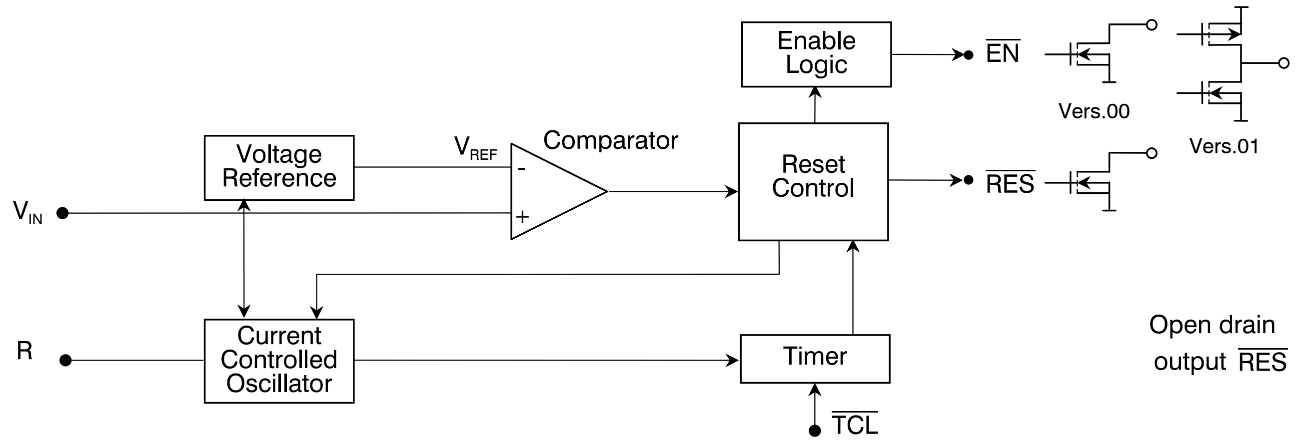


Fig. 8

Pin Description

Pin	Name	Function
1	$\overline{EN}$	**Vers. 00:** Open drain active low enable output. $\overline{EN}$ must be pulled up to V_{DD} even if unused. **Vers. 01:** Push-pull active low enable output
2	$\overline{RES}$	Open drain active low reset output. $\overline{RES}$ must be pulled up to V_{DD} even if unused
3	$\overline{TCL}$	Watchdog timer clear input signal
4	V_{SS}	GND terminal
5	NC	No connection
6	V_{DD}	Voltage supply
7	R	R_{EXT} input for RC oscillator tuning
8	V_{IN}	Voltage comparator input

Table 5

Functional Description

V_{IN} Monitoring

The power-on reset and the power-down reset are generated as a response to the external voltage level applied on the V_{IN} input.The V_{DD} voltage at which reset is asserted or released is determined by the external voltage divider between V_{DD} and V_{SS}, as shown on Fig. 9. A part of V_{DD} is compared to the internal voltage reference. To determine the values of the divider, the leakage current at V_{IN} must be taken into account, as well as the current consumption of the divider itself. Low resistor values will need more current, but high resistor values will make the reset threshold less accurate at high temperature, due to a possible leakage current at the V_{IN} input. The sum of the two resistors should stay below 300 kΩ. The formula is: $V_{RESET} = V_{REF} *(1 + R_1/R_2)$. Example: choosing R_1 = 100 kΩ and R_2 = 51 kΩ will result in a V_{DD} reset threshold of 4.5 V (typ.).

At power-up the reset output ($\overline{RES}$) is held low (see Fig. 5). When V_{IN} becomes greater than V_{REF}, the $\overline{RES}$ output is held low for an additional power-on reset (POR) delay which is equal to the watchdog time T_{WD} (typically 100 ms with an external resistor of 123 kΩ connected at R pin). The POR delay prevents repeated toggling of RES even if V_{IN} and the INPUT voltage drops out and recovers. The POR delay allows the microprocessor's crystal oscillator time to start and stabilize and ensures correct recognition of the reset signal to the microprocessor.

The $\overline{RES}$ output goes active low generating the power-down reset whenever V_{IN} falls below V_{REF}. The sensitivity or reaction time of the internal comparator to the voltage level on V_{IN} is typically 5 μs.

Timer Programming

The on-chip oscillator with an external resistor R_{EXT} connected between the R pin and V_{SS} (see Fig. 9) allows the user to adjust the power-on reset (POR) delay, watchdog time T_{WD} and with this also the closed and open time windows as well as the watchdog reset pulse width (T_{WD}/40).

With R_{EXT} = 123 kΩ, the typical delays are:

- Power-on reset delay: T_{POR} is 100 ms
- Watchdog time: T_{WD} is 100 ms
- Closed window: T_{CW} is 80 ms
- Open window: T_{OW} is 40 ms
- Watchdog reset: T_{WDR} is 2.5 ms

Note the current consumption increases as the frequency increases.

Watchdog Timeout Period Description

The watchdog timeout period is divided into two parts, a "closed" window and an "open" window (see Fig. 4) and is defined by two parameters, T_{WD} and the Open Window Percentage (OWP).

The closed window starts just after the watchdog timer resets and is defined by $T_{CW} = T_{WD} - OWP(T_{WD})$.

The open window starts after the closed time window finishes and lasts till $T_{WD} + OWP(T_{WD})$. The open window time is defined by $T_{OW} = 2 \times OWP(T_{WD})$.

For example if T_{WD} = 100 ms (actual value) and OWP = ± 20% this means the closed window lasts during first the 80 ms (T_{CW} = 80 ms = 100 ms – 0.2 (100 ms)) and the open window the next 40 ms (T_{OW} = 2 x 0.2 (100 ms) = 40 ms). The watchdog can be serviced between 80 ms and 120 ms after the timer reset. However as the time base is ± 10% accurate, software must use the following calculation as the limits for servicing signal $\overline{\text{TCL}}$ during the open window:

Related to curves (Fig. 10 to Fig. 20), especially Fig. 19 and Fig. 20, the relation between T_{WD} and R_{EXT} could easily be defined. Let us take an example describing the variations due to production and temperature:

1. Choice, T_{WD} = 26 ms.
2. Related to Fig. 20, the coefficient (T_{WD} to R_{EXT}) is 1.155 where R_{EXT} is in kΩ and T_{WD} in ms.
3. R_{EXT} (typ.) = 26 x 1.155 = 30.0 kΩ.
4. 26 ms at +25 °C

[a](26 – 10% = 23.4 ms) (26 + 10% = 28.6 ms)[a]

[b](23.4 – 5% = 22.2 ms) (28.6 + 5% = 30.0 ms)[b]

min.: (30.0 – 20% = 24.0 ms) max.: (22.2 + 20% = 26.7 ms)

Typical $\overline{\text{TCL}}$ period of (24.0 + 26.7) / 2 = 25.4 ms

The ratio between T_{WD} = 26 ms and the ($\overline{\text{TCL}}$ period) = 25.4 ms is 0.975.

Then the relation over the production and the full temperature range is, $\overline{\text{TCL}}$ period = 0.975 x T_{WD} or

$$\overline{\text{TCL}}\text{ period} = \frac{0.975 \times R_{EXT}}{1.155}$$, as typical value.

a) While PRODUCTION value unknown for the customer when $R_{EXT} \neq 123$ kΩ.

b) While operating TEMPERATURE range −40 °C ≤ T_A ≤ +85 °C.

5. If you fixed a $\overline{\text{TCL}}$ period = 26 ms

$$\Rightarrow R_{EXT} = \frac{26 \times 1.155}{0.975} = 30.8\ \text{k}\Omega.$$

If during your production the T_{WD} time can be measured at T_A = +25 °C and the μC can adjust the $\overline{\text{TCL}}$ period, then the $\overline{\text{TCL}}$ period range will be much larger for the full operating temperature.

Timer Clearing and $\overline{\text{RES}}$ Action

The watchdog circuit monitors the activity of the processor. If the user's software does not send a pulse to the $\overline{\text{TCL}}$ input within the programmed open window timeout period, a short watchdog $\overline{\text{RES}}$ pulse is generated which is equal to T_{WD}/40 = 2.5 ms typically (see Fig. 6).

With the open window constraint, new security is added to conventional watchdogs by monitoring both software cycle time and execution. Should software clear the watchdog too quickly (incorrect cycle time) or too slowly (incorrect execution), it will cause the system to be reset. If the software is stuck in a loop which includes the routine to clear the watchdog, then a conventional watchdog would not make a system even though the software is malfunctioning; the V6150 would make a system reset because the watchdog would be cleared too quickly.

If no $\overline{\text{TCL}}$ pulse is applied before the closed and open windows expire, $\overline{\text{RES}}$ will start to generate square waves of period – $T_{CW} + T_{OW} + T_{WDR}$. The watchdog will remain in this state until the next $\overline{\text{TCL}}$ falling edge appears during an open window, or until a fresh power-up sequence. The system enable output, $\overline{\text{EN}}$, can be used to prevent critical control functions being activated in the event of the system going into this failure mode (see section "Enable – $\overline{\text{EN}}$ Output").

The $\overline{\text{RES}}$ output must be pulled up to V_{DD} even if the output is not used by the system (see Fig. 9).

Combined Voltage and Timer Action

The combination of voltage and timer actions is illustrated by the sequence of events shown in Fig. 7. On power-up, when the voltage at V_{IN} reaches V_{REF}, the power-on-reset, POR, delay is initialized and holds $\overline{\text{RES}}$ active for the time of the POR delay. A $\overline{\text{TCL}}$ pulse will have no effect until this power-on-reset delay is completed. When the risk exists that $\overline{\text{TCL}}$ temporarily floats, e.g. during T_{POR}, a pull-up to V_{DD} is required on that pin. After the POR delay has elapsed, $\overline{\text{RES}}$ goes inactive and the watchdog timer starts acting. If no $\overline{\text{TCL}}$ pulse occurs, $\overline{\text{RES}}$ goes active low for a short time T_{WDR} after each closed and open window period. A $\overline{\text{TCL}}$ pulse coming during the open window clears the watchdog timer. When the $\overline{\text{TCL}}$ pulse occurs too early (during the closed window), $\overline{\text{RES}}$ goes active and a new timeout sequence starts. A voltage drop below the V_{REF} level for longer than typically 5 μs, overrides the timer and immediately forces $\overline{\text{RES}}$ active and $\overline{\text{EN}}$ inactive. Any further $\overline{\text{TCL}}$ pulse has no effect until the next power-up sequence has completed.

Enable – $\overline{\text{EN}}$ Output

The system enable output, $\overline{\text{EN}}$, is inactive always when $\overline{\text{RES}}$ is active and remains inactive after a $\overline{\text{RES}}$ pulse until the watchdog is serviced correctly 3 consecutive times (ie. the $\overline{\text{TCL}}$ pulse must come in the open window). After three consecutive services of the watchdog with $\overline{\text{TCL}}$ during the open window, the $\overline{\text{EN}}$ goes active low.

A malfunctioning system would be repeatedly reset by

the watchdog. In a conventional system critical motor controls could be energized each time reset goes inactive (time allowed for the system to restart) and in this way the electrical motors driven by the system could function out of control. The V6150 prevents the above failure mode by using the $\overline{EN}$ output to disable the motor controls until software has successfully cleared the watchdog three times (i.e. the system has correctly restarted after a reset condition).
For the version 00 the $\overline{EN}$ output must be pulled up to V_{DD} even if the output is not used by the system (see Fig.9).

Typical Application

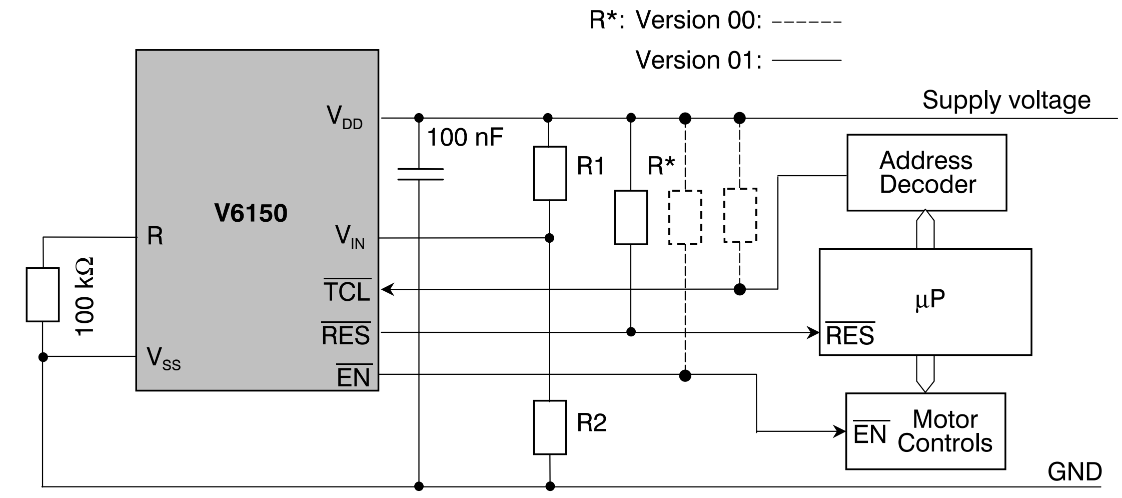


Fig. 9

T_{WD} versus Temperature at 5 V

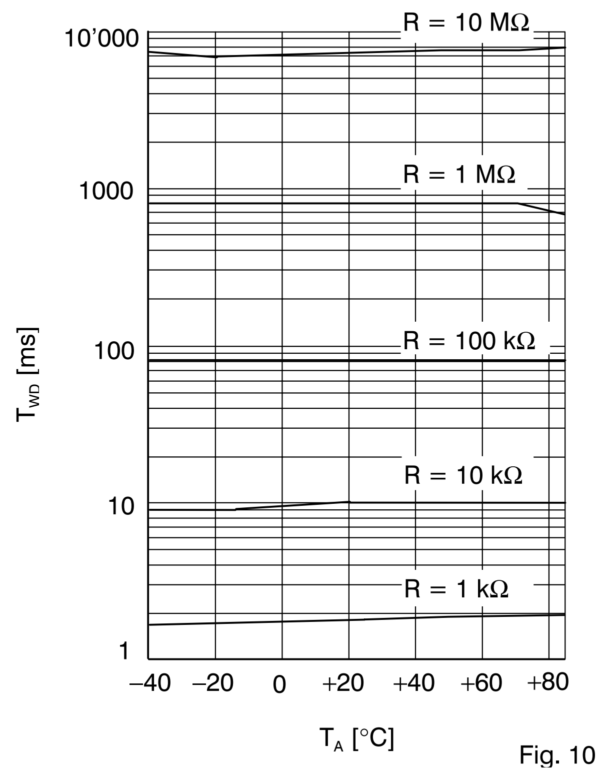


Fig. 10

T_{WD} versus R at 5 V

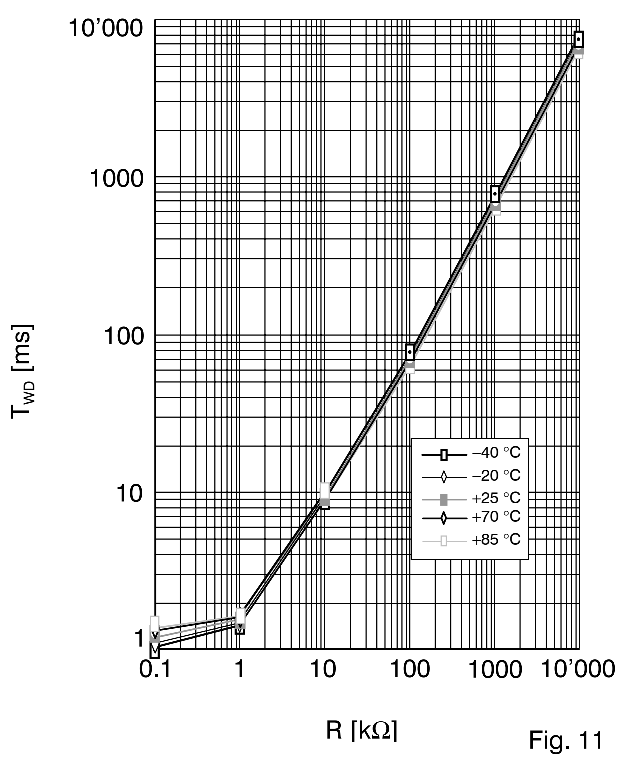


Fig. 11

T_{WD} versus V_{DD} at T_A = +25 °C

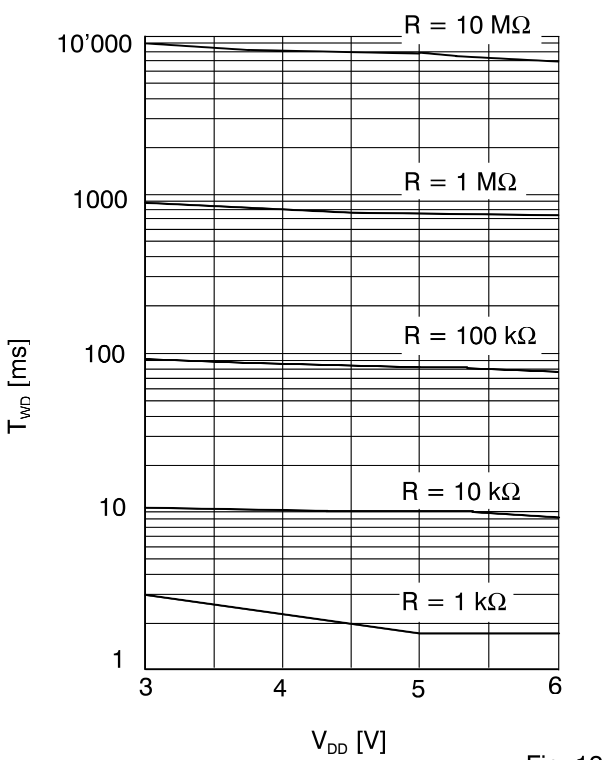


Fig. 12

T_{WD} versus R at T_A = +25 °C

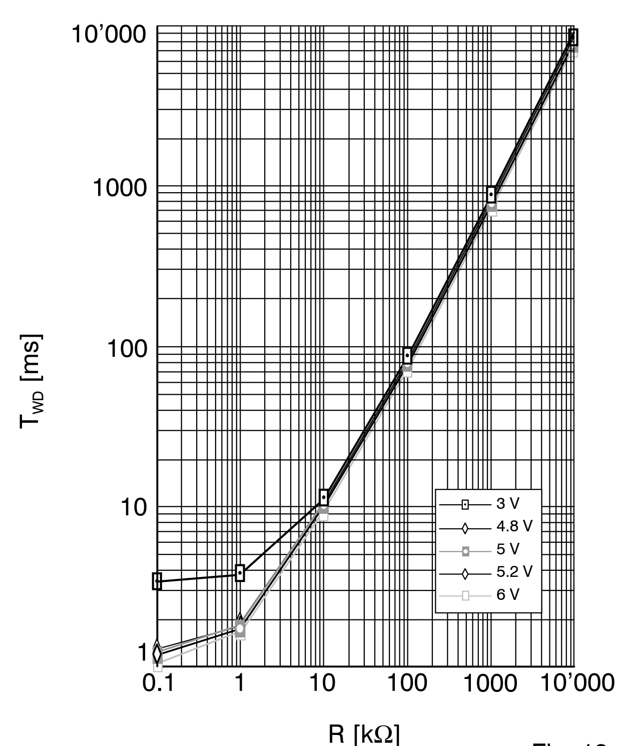


Fig. 13

T_{WD} versus R at T_A = +25 °C

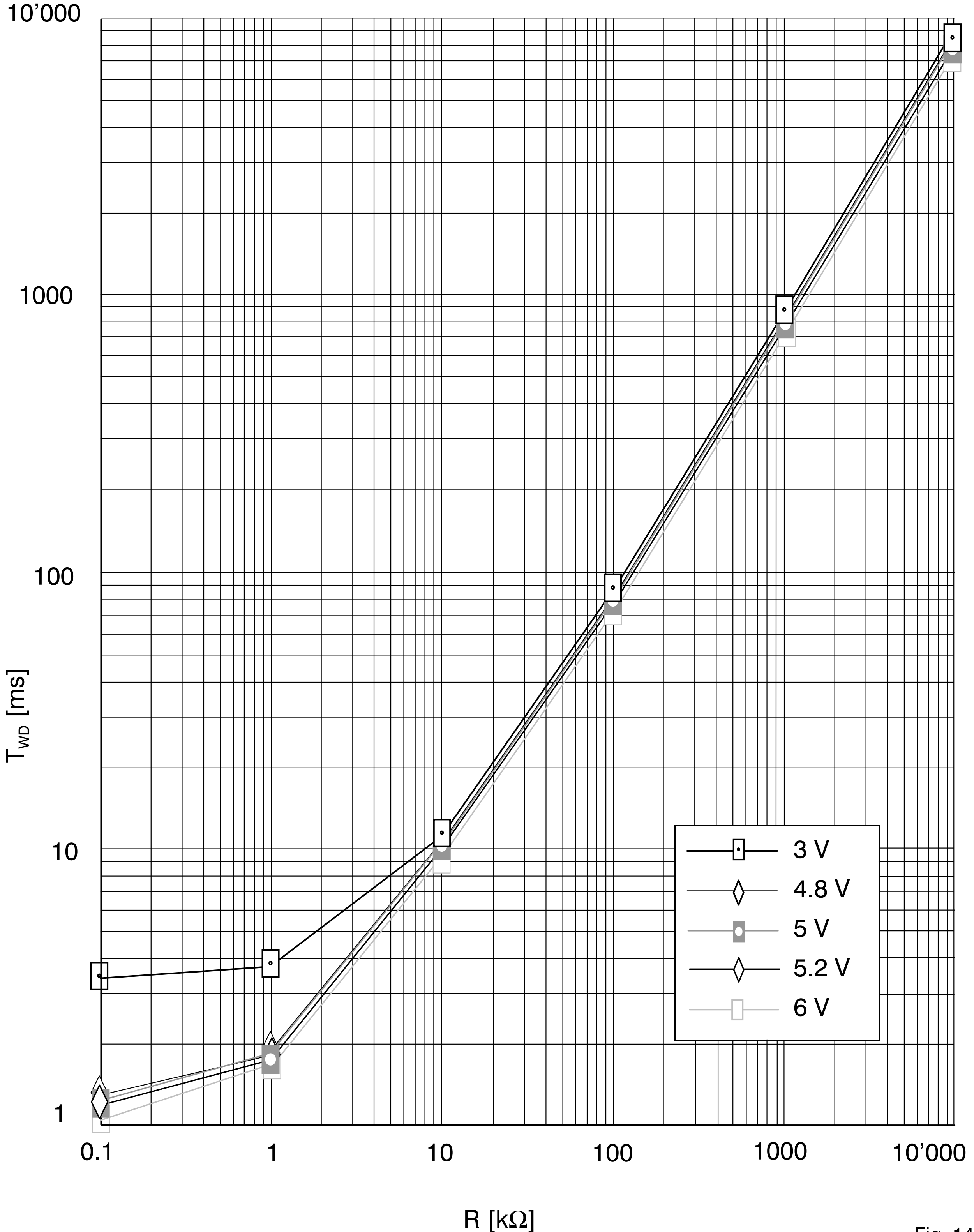


Fig. 14

T_{WD} versus V_{DD} at T_A = +85 °C

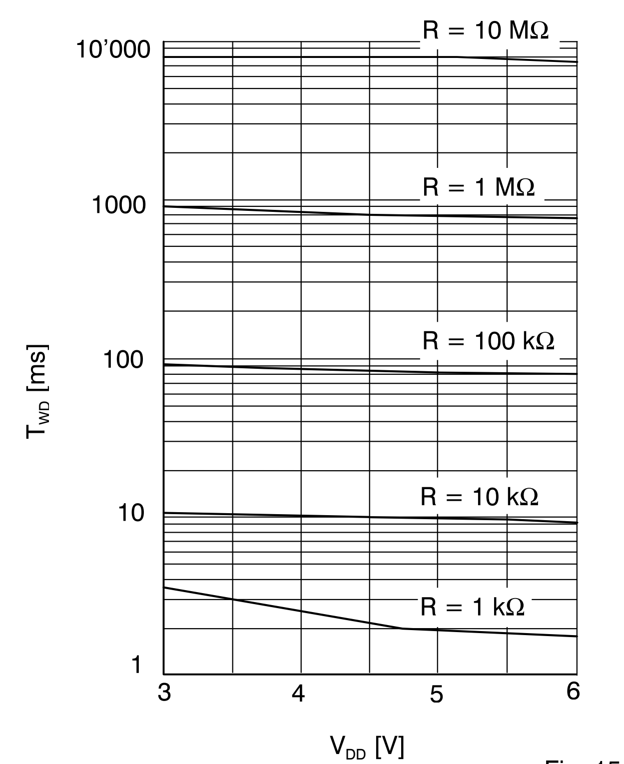


Fig. 15

T_{WD} versus R at T_A = +85 °C

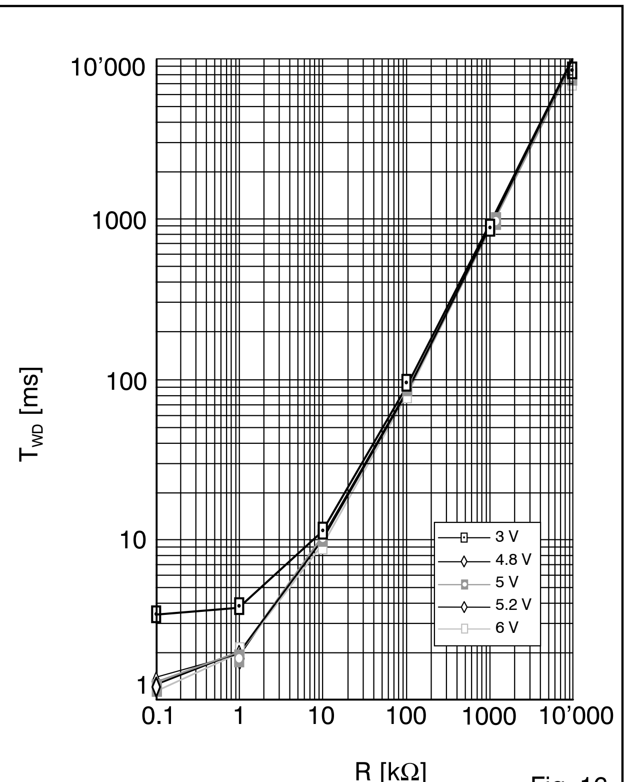


Fig. 16

T_{WD} versus V_{DD} at T_A = –40 °C

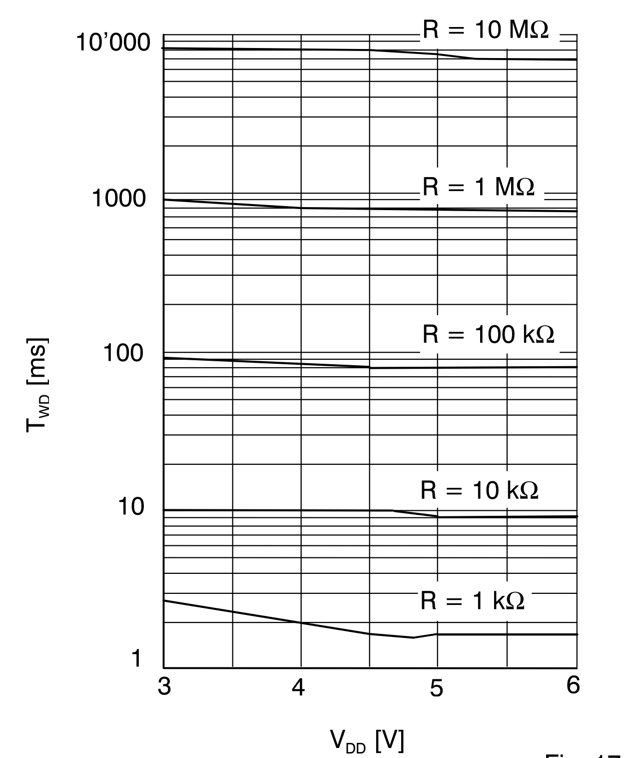


Fig. 17

T_{WD} versus R at T_A = –40 °C

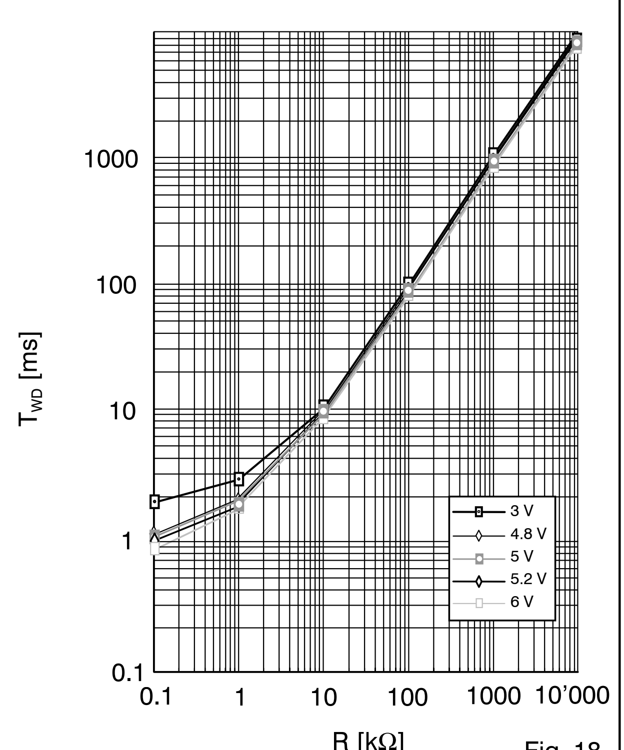


Fig. 18

T_{WD} Coefficient versus R_{EXT} at T_A = +25 °C

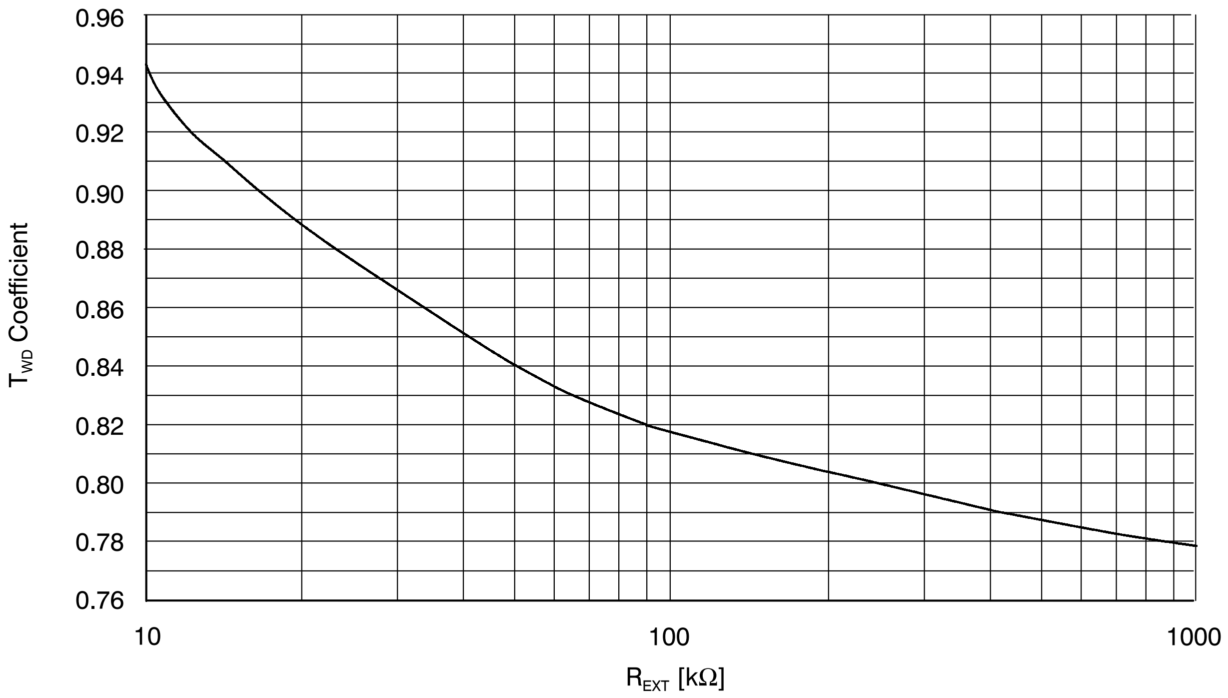


Fig. 19

R_{EXT} Coefficient versus T_{WD} at T_A = +25 °C

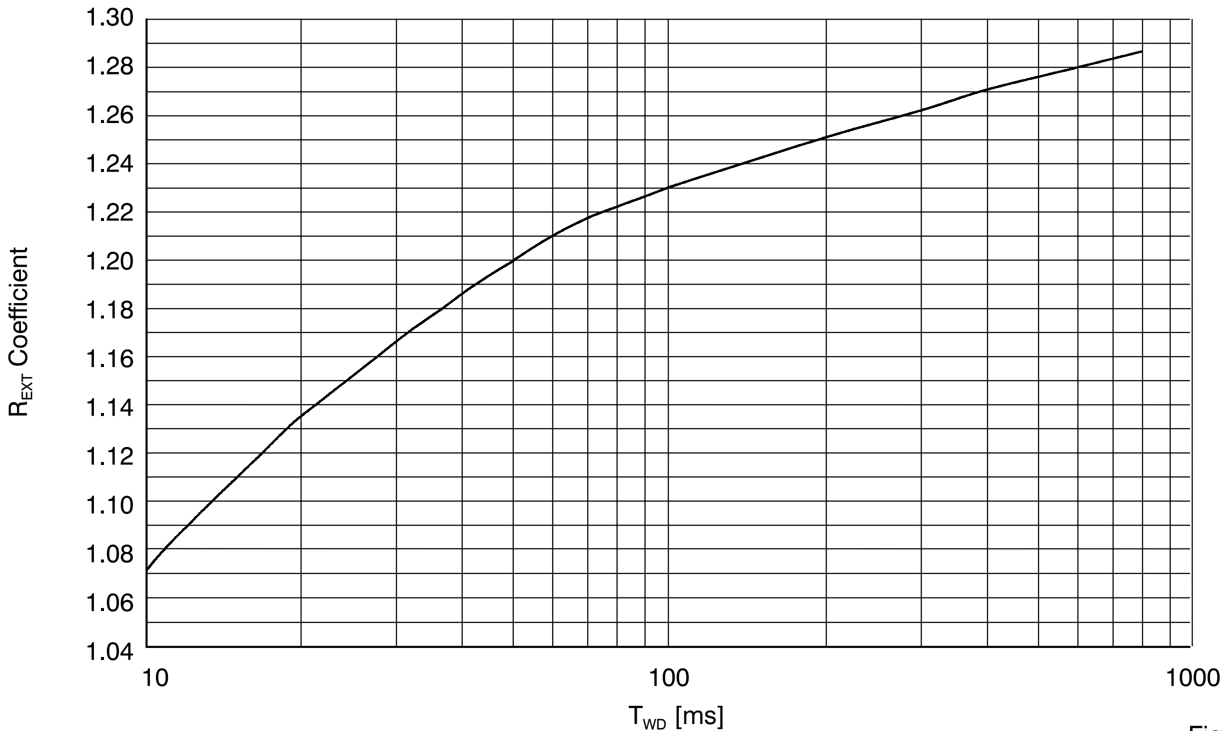
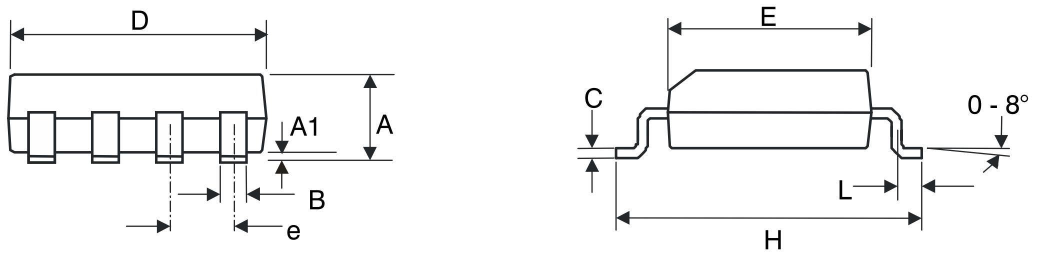
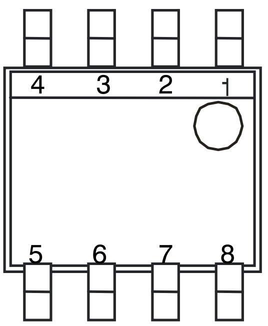


Fig. 20

Package Information

Dimensions of 8-Pin SOIC Package



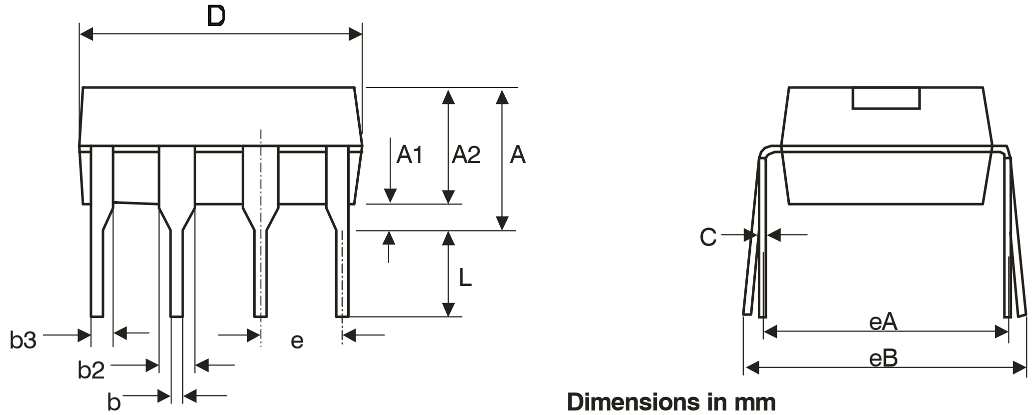


Dimensions in mm

	Min	Nom	Max
A	1.35	1.63	1.75
A1	0.10	0.15	0.25
B	0.33	0.41	0.51
C	0.19	0.20	0.25
D	4.80	4.93	5.00
E	3.80	3.94	4.00
e		1.27	
H	5.80	5.99	6.20
L	0.40	0.64	1.27

Fig.21

Dimensions of 8-Pin Plastic DIP Package



Dimensions in mm

	Min.	Nom.	Max.
A			5.33
A1	0.38		
A2	2.92	3.30	4.95
b	0.35	0.45	0.56
b2	1.14	1.52	1.78
b3	0.76	0.99	1.14
C	0.20	0.25	0.35

	Min.	Nom.	Max.
D	9.01	9.27	10.16
E	7.62	7.87	8.25
E1	6.09	6.35	7.11
e		2.54	
eA		7.62	
eB			10.92
L	2.92	3.30	3.81

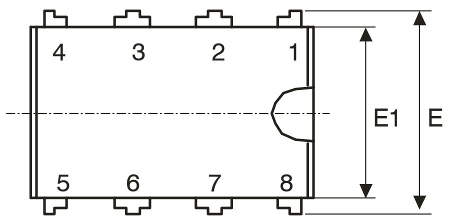


Fig. 22

Ordering Information

When ordering, please specify complete Part Number

Part Number	Output EN	Temperature Range	Package	Delivery Form	Package Marking (first line)
V6150V01SO8A	Push-pull	-40 °C to +85 °C	8-pin SOIC	Stick	615001
V6150V01SO8B			8-pin SOIC	Tape & Reel	615001
V6150V01DL8A*			8-pin plastic DIP	Stick	V615001
V6150V00SO8A*	Open drain		8-pin SOIC	Stick	615000
V6150V00SO8B*			8-pin SOIC	Tape & Reel	615000
V6150V00DL8A*			8-pin plastic DIP	Stick	V615000
V6150V01XSO8A*	Push-pull	-40 °C to +125 °C	8-pin SOIC	Stick	6150V1X
V6150V01XSO8B*			8-pin SOIC	Tape & Reel	6150V1X
V6150V01XDL8A*			8-pin plastic DIP	Stick	V615001X
V6150V00XSO8A*	Open drain		8-pin SOIC	Stick	6150V0X
V6150V00XSO8B*			8-pin SOIC	Tape & Reel	6150V0X
V6150V00XDL8A*			8-pin plastic DIP	Stick	V615000X

* = non-stock items. Might be available on request and upon minimum order quantity (please contact EM Microelectronic).